

***LCFC Confidential***  
***Dooku/Jinn 2.0***  
***E490S/E490/R490/E590/R590***  
***NM-911 Rev0.4 Schematic***

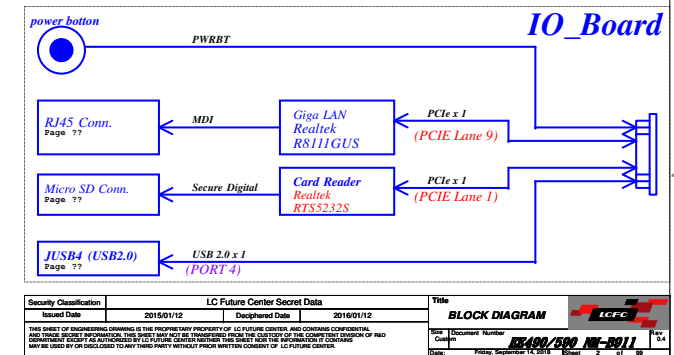
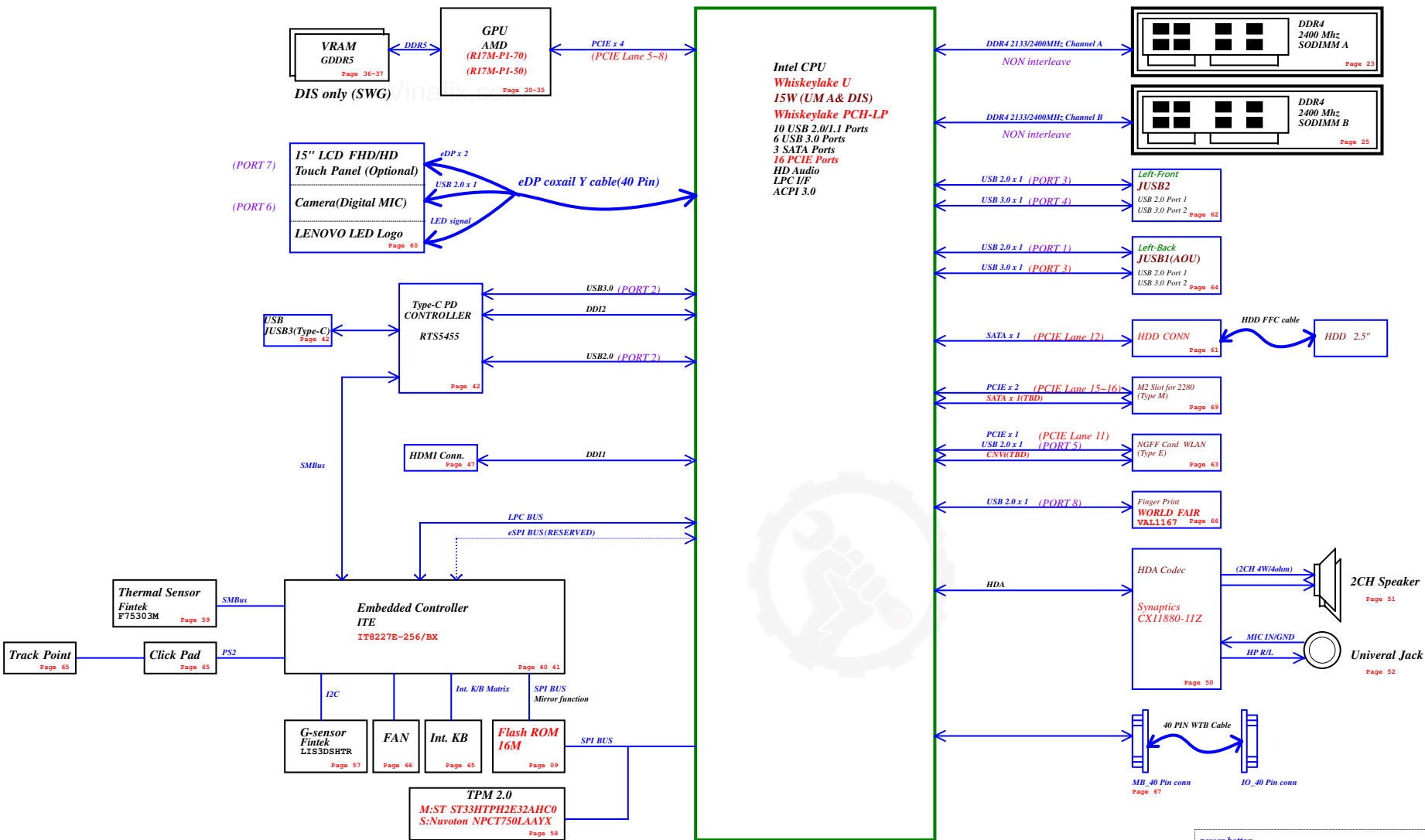
***Intel Whiskey Processor with DDR4 + PCH***

***R17M-P1-50***

***R17M-P1-70***

***2018-09-21 Rev0.4***

Security Classification	LC Future Center Secret Data			Title	
Issued Date	2015/01/12	Deciphered Date	2016/01/12	COVER PAGE	
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## Voltage Rails

O --> Means ON  
X --> Means OFF

Power Plane / State	B+	+1.05VALW +3VALW +1.8VALW +5VALW	+1.2V +0.6VS +VCC_ST	+5VS +3VS +VCC_CORE +VCC_GT +VCC_SA +VCC_IO +VCC_STG +VGA_CORE +1.5VS +0.95VS_VGA +1.5VS_VGA +1.8VS_VGA +3VS_VGA
S0	O	O	O	O
S3	O	O	O	X
S5 S4/AC Only	O	O	X	X
S5 S4 Battery only	O	X	X	X
S5 S4 AC & Battery don't exist	X	X	X	X

STATE	SIGNAL						
	SLP_A#	SLP_S3#	SLP_S4#	SLP_S5#	VM_PWRON	EC_ON	SUSP#
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON
S1 (Power on)	HIGH	HIGH	HIGH	HIGH	ON	ON	ON
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	ON	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	ON	OFF

## SMBUS Control Table

	SOURCE	Main VGA	BATT	SODIMM	WLAN WiMAX	Thermal Sensor	PCH	CP Module	Security ROM	LAN PHY
EC_SMB_CK1 EC_SMB_DA1	IT8586E +3VL	X	V +3VALW	X	X	X	X	X	X	X
EC_SMB_CK3 EC_SMB_DA3	IT8586E +3VS	V +3VS_VGA	X	X	X	V +3VS	V +3V_PCH	X	X	X
PCH_SMB_CLK PCH_SMB_DATA	PCH +3V_PCH	X	X	V +3VS	V +3VS	V +3VS	X	V +5VS	V +3VS	X
PCH_SML0_CLK PCH_SML0_DATA	PCH +3V_PCH	X	X	X	X	X	X	X	X	V +3VALW

## HSIO Port

Port	Device
1	PCIE (Card Reader)
2	Type-C Port
3	Type-A Port Gen1 (AOU)
4	Type-A Port Gen2 (DCI)
5	PCIE (GPU)
6	PCIE (GPU)
7	PCIE (GPU)
8	PCIE (GPU)
9	PCIE (LAN)
10	N/A
11	PCIE (WLAN)
12	SATA express (SATA)
13	N/A
14	N/A
15	M.2 (PCIE)
16	M.2 (SATA)


## USB2.0 Port

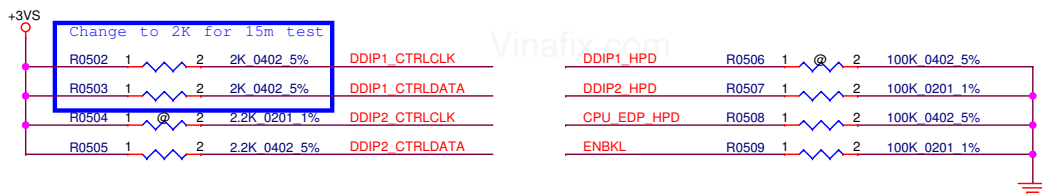
Port	Device
1	Type-A Port Gen1 (AOU)
2	Type-C Port
3	Type-A Port Gen2 (DCI)
4	USB port (Sub Board)
5	BT
6	Camera
7	Touch Panel
8	Finger Printer
9	N/A
10	N/A

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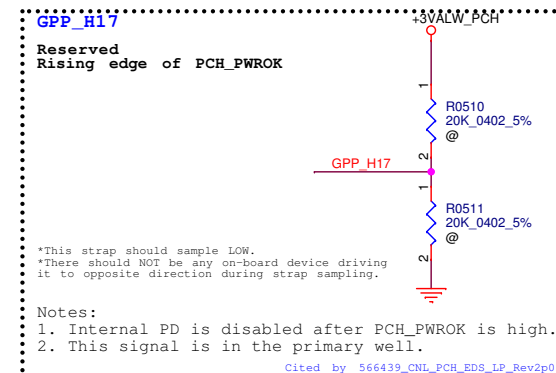
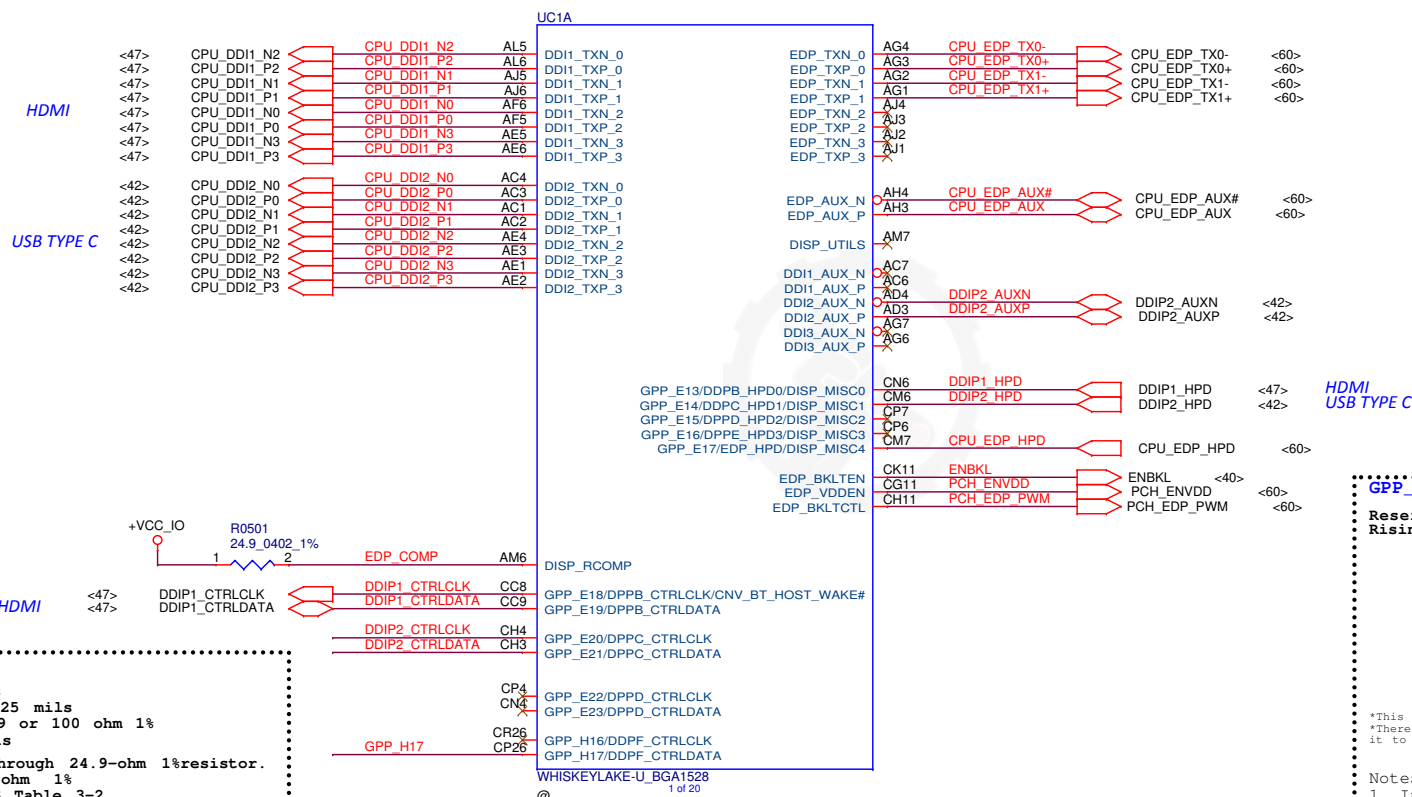
**BOM Structure Table**

BOM Structure	NOTE
PCB@	For PCB load BOM
3G@	3G function with WWAN
DIS@	Discreate SKU
UMA@	UMA SKU
DPRE@	With DP re-driver
NODPRE@	Bypass DP re-driver
NVPRO@	For Non-VPRO function
VPRO@	For VPRO function
MIRROR@	For mirror function
TPM@	TPM function
X76@	GPU VRAM Setting
XDP@	XDP function
EXO@	EXO function
ME@	ME Connector
EMC@	For EMC function
EMC_NS@	For EMC function (no mount)
RF@	For RF function
RF_NS@	For RF function (no mount)
WHL@	For WHL SKU
CNL@	For CNL SKU
SW@/AUDIO@	For Audio Jack Debug Selection
14S@	To recognize 14S SKU
CD@	Reduce capacitors quantity

Security Classification		LC Future Center Secret Data		Title			
Issued Date	2015/01/12	Deciphered Date	2016/01/12	BOM LIST			
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DP port	Enable	Disable
DDPB_CTRLDATA	Pull up to 3.3 V with 2.2-k ohm $\pm$ 5% resistor	no connect
DDPC_CTRLDATA	Pull up to 3.3 V with 2.2-k ohm $\pm$ 5% resistor	no connect




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eDP_RCOMP
Trace Width: 5 mils
Isolation Spacing: 25 mils
Resistor Value: 24.9 or 100 ohm 1%
Max Length: 600 mils
Pull-up to VCCIO through 24.9-ohm 1%resistor.
For CNL, it is 100 ohm 1%
Please refer to PDG Table 3-2.

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Cited by 575412\_WHL\_U\_PDG\_Rev0.9

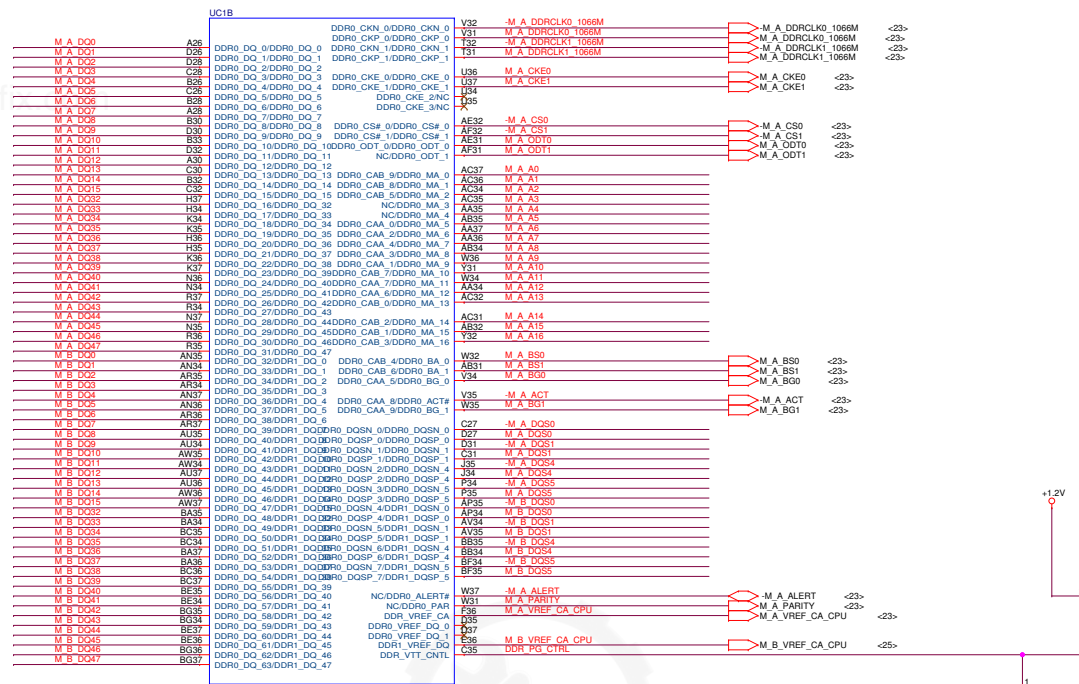
Security Classification		LC Future Center Secret Data		Title		
Issued Date	2015/01/12	Deciphered Date	2016/01/12	<b>WHL(A)_DDI/eDP</b>		
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TABLE

	Pin	Interleave	Non-Interleave
Block 0	A26	DDR0_DQ[0]	DDR0_DQ[0]
	D26	DDR0_DQ[1]	DDR0_DQ[1]
	D28	DDR0_DQ[2]	DDR0_DQ[2]
	C28	DDR0_DQ[3]	DDR0_DQ[3]
	B26	DDR0_DQ[4]	DDR0_DQ[4]
	C26	DDR0_DQ[5]	DDR0_DQ[5]
	B28	DDR0_DQ[6]	DDR0_DQ[6]
	A28	DDR0_DQ[7]	DDR0_DQ[7]
	B30	DDR0_DQ[8]	DDR0_DQ[8]
	D30	DDR0_DQ[9]	DDR0_DQ[9]
	B33	DDR0_DQ[10]	DDR0_DQ[10]
	D32	DDR0_DQ[11]	DDR0_DQ[11]
	A30	DDR0_DQ[12]	DDR0_DQ[12]
	C30	DDR0_DQ[13]	DDR0_DQ[13]
	B32	DDR0_DQ[14]	DDR0_DQ[14]
	C32	DDR0_DQ[15]	DDR0_DQ[15]
Block 2	H37	DDR0_DQ[16]	DDR0_DQ[32]
	H34	DDR0_DQ[17]	DDR0_DQ[33]
	K34	DDR0_DQ[18]	DDR0_DQ[34]
	K35	DDR0_DQ[19]	DDR0_DQ[35]
	H36	DDR0_DQ[20]	DDR0_DQ[36]
	H35	DDR0_DQ[21]	DDR0_DQ[37]
	K36	DDR0_DQ[22]	DDR0_DQ[38]
	K37	DDR0_DQ[23]	DDR0_DQ[39]
	N36	DDR0_DQ[24]	DDR0_DQ[40]
	N34	DDR0_DQ[25]	DDR0_DQ[41]
	R37	DDR0_DQ[26]	DDR0_DQ[42]
	R34	DDR0_DQ[27]	DDR0_DQ[43]
	N37	DDR0_DQ[28]	DDR0_DQ[44]
	N35	DDR0_DQ[29]	DDR0_DQ[45]
	R36	DDR0_DQ[30]	DDR0_DQ[46]
	R35	DDR0_DQ[31]	DDR0_DQ[47]
Block 4	AN35	DDR0_DQ[32]	DDR1_DQ[0]
	AN34	DDR0_DQ[33]	DDR1_DQ[1]
	AR35	DDR0_DQ[34]	DDR1_DQ[2]
	AR34	DDR0_DQ[35]	DDR1_DQ[3]
	AN37	DDR0_DQ[36]	DDR1_DQ[4]
	AN36	DDR0_DQ[37]	DDR1_DQ[5]
	AR36	DDR0_DQ[38]	DDR1_DQ[6]
	AR37	DDR0_DQ[39]	DDR1_DQ[7]
	AU35	DDR0_DQ[40]	DDR1_DQ[8]
	AU34	DDR0_DQ[41]	DDR1_DQ[9]
	AW35	DDR0_DQ[42]	DDR1_DQ[10]
	AW34	DDR0_DQ[43]	DDR1_DQ[11]
	AU36	DDR0_DQ[44]	DDR1_DQ[12]
	AW36	DDR0_DQ[45]	DDR1_DQ[13]
	AW37	DDR0_DQ[46]	DDR1_DQ[14]
Block 6	BA35	DDR0_DQ[48]	DDR1_DQ[32]
	BA34	DDR0_DQ[49]	DDR1_DQ[33]
	BC35	DDR0_DQ[50]	DDR1_DQ[34]
	BC34	DDR0_DQ[51]	DDR1_DQ[35]
	BA37	DDR0_DQ[52]	DDR1_DQ[36]
	BA36	DDR0_DQ[53]	DDR1_DQ[37]
	BC36	DDR0_DQ[54]	DDR1_DQ[38]
	BC37	DDR0_DQ[55]	DDR1_DQ[39]
	BE35	DDR0_DQ[56]	DDR1_DQ[40]
	BE34	DDR0_DQ[57]	DDR1_DQ[41]
	BG35	DDR0_DQ[58]	DDR1_DQ[42]
	BG34	DDR0_DQ[59]	DDR1_DQ[43]
	BE37	DDR0_DQ[60]	DDR1_DQ[44]
	BE36	DDR0_DQ[61]	DDR1_DQ[45]
	BG36	DDR0_DQ[62]	DDR1_DQ[46]
	BG37	DDR0_DQ[63]	DDR1_DQ[47]

↑  
LOGIC



TABLE

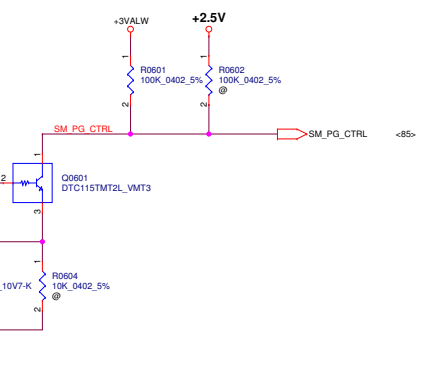
	Pin	Interleave	Non-Interleave
Block 0	C27	DDR0_DQSN[0]	DDR0_DQSN[0]
	D27	DDR0_DQSP[0]	DDR0_DQSP[0]
	D31	DDR0_DQSN[1]	DDR0_DQSN[1]
	C31	DDR0_DQSP[1]	DDR0_DQSP[1]
Block 2	J35	DDR0_DQSN[2]	DDR0_DQSN[4]
	J34	DDR0_DQSP[2]	DDR0_DQSP[4]
	P34	DDR0_DQSN[3]	DDR0_DQSN[5]
	P35	DDR0_DQSP[3]	DDR0_DQSP[5]
Block 4	AP35	DDR0_DQSN[4]	DDR1_DQSN[0]
	AP34	DDR0_DQSP[4]	DDR1_DQSP[0]
	AV34	DDR0_DQSN[5]	DDR1_DQSN[1]
	AV35	DDR0_DQSP[5]	DDR1_DQSP[1]
Block 6	BB35	DDR0_DQSN[6]	DDR1_DQSN[4]
	BB34	DDR0_DQSP[6]	DDR1_DQSP[4]
	BF34	DDR0_DQSN[7]	DDR1_DQSN[5]
	BF35	DDR0_DQSP[7]	DDR1_DQSP[5]

↑  
LOGIC

TABLE

Pin	DDR3L	LPDDR3	DDR4
AB35	DDR0_MA[5]	DDR0_CAA[0]	DDR0_MA[5]
W36	DDR0_MA[9]	DDR0_CAA[1]	DDR0_MA[9]
AA37	DDR0_MA[6]	DDR0_CAA[2]	DDR0_MA[6]
AB34	DDR0_MA[8]	DDR0_CAA[3]	DDR0_MA[8]
AA36	DDR0_MA[7]	DDR0_CAA[4]	DDR0_MA[7]
V34	DDR0_BA[2]	DDR0_CAA[5]	DDR0_BG[0]
AA34	DDR0_MA[12]	DDR0_CAA[6]	DDR0_MA[12]
W34	DDR0_MA[11]	DDR0_CAA[7]	DDR0_MA[11]
V35	DDR0_MA[15]	DDR0_CAA[8]	DDR0_ACT#
W35	DDR0_MA[14]	DDR0_CAA[9]	DDR0_BG[1]
AC32	DDR0_MA[13]	DDR0_CAB[0]	DDR0_MA[13]
AB32	DDR0_CAS#	DDR0_CAB[1]	DDR0_MA[15]
AC31	DDR0_WE#	DDR0_CAB[2]	DDR0_MA[14]
Y32	DDR0_RAS#	DDR0_CAB[3]	DDR0_MA[16]
W32	DDR0_BA[0]	DDR0_CAB[4]	DDR0_BA[0]
AC34	DDR0_MA[2]	DDR0_CAB[5]	DDR0_MA[2]
AB31	DDR0_BA[1]	DDR0_CAB[6]	DDR0_BA[1]
Y31	DDR0_MA[10]	DDR0_CAB[7]	DDR0_MA[10]
AC36	DDR0_MA[1]	DDR0_CAB[8]	DDR0_MA[1]
AC37	DDR0_MA[0]	DDR0_CAB[9]	DDR0_MA[0]
AC35	DDR0_MA[3]	Not Used	DDR0_MA[3]
AA35	DDR0_MA[4]	Not Used	DDR0_MA[4]

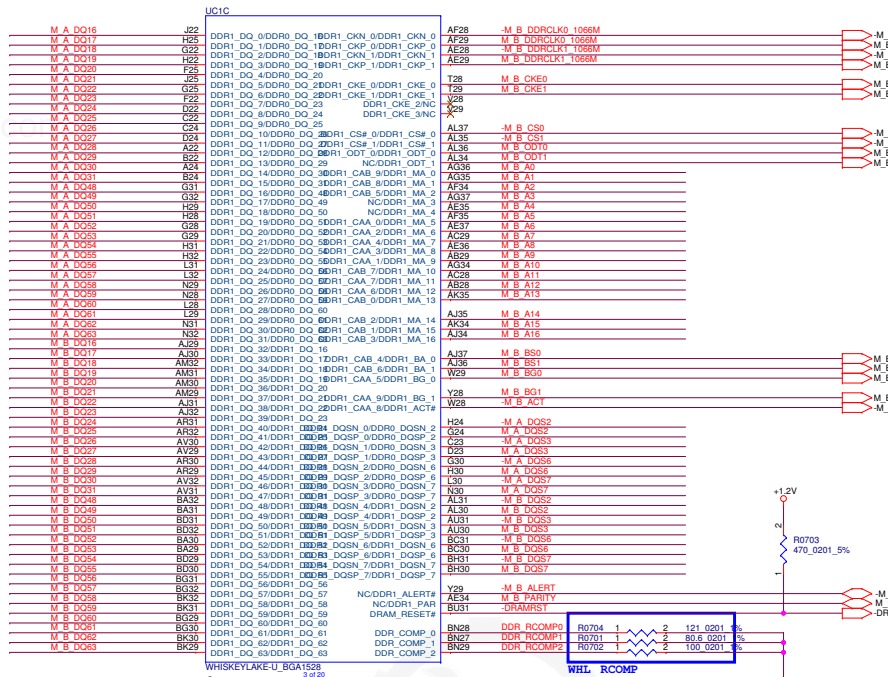
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LOGIC



TABLE

	Pin	Interleave	Non-Interleave
Block 1	J22	DDR1_DQ[0]	DDR0_DQ[16]
	H25	DDR1_DQ[1]	DDR0_DQ[17]
	G22	DDR1_DQ[2]	DDR0_DQ[18]
	H22	DDR1_DQ[3]	DDR0_DQ[19]
	F25	DDR1_DQ[4]	DDR0_DQ[20]
	J25	DDR1_DQ[5]	DDR0_DQ[21]
	G25	DDR1_DQ[6]	DDR0_DQ[22]
	F22	DDR1_DQ[7]	DDR0_DQ[23]
	D22	DDR1_DQ[8]	DDR0_DQ[24]
	C22	DDR1_DQ[9]	DDR0_DQ[25]
	C24	DDR1_DQ[10]	DDR0_DQ[26]
	D24	DDR1_DQ[11]	DDR0_DQ[27]
	A22	DDR1_DQ[12]	DDR0_DQ[28]
	B22	DDR1_DQ[13]	DDR0_DQ[29]
	A24	DDR1_DQ[14]	DDR0_DQ[30]
	B24	DDR1_DQ[15]	DDR0_DQ[31]
Block 3	G31	DDR1_DQ[16]	DDR0_DQ[48]
	G32	DDR1_DQ[17]	DDR0_DQ[49]
	H29	DDR1_DQ[18]	DDR0_DQ[50]
	H28	DDR1_DQ[19]	DDR0_DQ[51]
	G28	DDR1_DQ[20]	DDR0_DQ[52]
	G29	DDR1_DQ[21]	DDR0_DQ[53]
	H31	DDR1_DQ[22]	DDR0_DQ[54]
	H32	DDR1_DQ[23]	DDR0_DQ[55]
	L31	DDR1_DQ[24]	DDR0_DQ[56]
	L32	DDR1_DQ[25]	DDR0_DQ[57]
	N29	DDR1_DQ[26]	DDR0_DQ[58]
	N28	DDR1_DQ[27]	DDR0_DQ[59]
	L28	DDR1_DQ[28]	DDR0_DQ[60]
	L29	DDR1_DQ[29]	DDR0_DQ[61]
	N31	DDR1_DQ[30]	DDR0_DQ[62]
	N32	DDR1_DQ[31]	DDR0_DQ[63]
Block 5	AJ29	DDR1_DQ[32]	DDR1_DQ[16]
	AJ30	DDR1_DQ[33]	DDR1_DQ[17]
	AM32	DDR1_DQ[34]	DDR1_DQ[18]
	AM31	DDR1_DQ[35]	DDR1_DQ[19]
	AM29	DDR1_DQ[36]	DDR1_DQ[20]
	AJ31	DDR1_DQ[37]	DDR1_DQ[21]
	AJ32	DDR1_DQ[38]	DDR1_DQ[22]
	AR31	DDR1_DQ[39]	DDR1_DQ[23]
	AR32	DDR1_DQ[40]	DDR1_DQ[24]
	AV30	DDR1_DQ[41]	DDR1_DQ[25]
	AV29	DDR1_DQ[42]	DDR1_DQ[26]
	AR30	DDR1_DQ[43]	DDR1_DQ[27]
	AR29	DDR1_DQ[44]	DDR1_DQ[28]
	AV32	DDR1_DQ[45]	DDR1_DQ[29]
	AV31	DDR1_DQ[46]	DDR1_DQ[30]
		DDR1_DQ[47]	DDR1_DQ[31]
Block 7	BA32	DDR1_DQ[48]	DDR1_DQ[48]
	BA31	DDR1_DQ[49]	DDR1_DQ[49]
	BD31	DDR1_DQ[50]	DDR1_DQ[50]
	BD32	DDR1_DQ[51]	DDR1_DQ[51]
	BA30	DDR1_DQ[52]	DDR1_DQ[52]
	BA29	DDR1_DQ[53]	DDR1_DQ[53]
	BD29	DDR1_DQ[54]	DDR1_DQ[54]
	BD30	DDR1_DQ[55]	DDR1_DQ[55]
	BG31	DDR1_DQ[56]	DDR1_DQ[56]
	BG32	DDR1_DQ[57]	DDR1_DQ[57]
	BK32	DDR1_DQ[58]	DDR1_DQ[58]
	BK31	DDR1_DQ[59]	DDR1_DQ[59]
	BG29	DDR1_DQ[60]	DDR1_DQ[60]
	BG30	DDR1_DQ[61]	DDR1_DQ[61]
	BK30	DDR1_DQ[62]	DDR1_DQ[62]
	BK29	DDR1_DQ[63]	DDR1_DQ[63]

LOGIC



[WHL PDG]for WHL DDR4 COMPENSATION  
DDR\_RCOMP[0] Pull down 121 ohm resistor  
DDR\_RCOMP[1] Pull down 80.6 ohm resistor  
DDR\_RCOMP[2] Pull down 100 ohm resistor

[WHL PDG]for CNL DDR4 COMPENSATION  
DDR\_RCOMP[0] Pull down 100 ohm resistor  
DDR\_RCOMP[1] Pull down 100 ohm resistor  
DDR\_RCOMP[2] Pull down 100 ohm resistor

TABLE

	Pin	Interleave	Non-Interleave
Block 1	H24	DDR1_DQSN[0]	DDR0_DQSN[2]
	G24	DDR1_DQSP[0]	DDR0_DQSP[2]
	C23	DDR1_DQSN[1]	DDR0_DQSN[3]
	D23	DDR1_DQSP[1]	DDR0_DQSP[3]
Block 3	G30	DDR1_DQSN[2]	DDR0_DQSN[6]
	H30	DDR1_DQSP[2]	DDR0_DQSP[6]
	L30	DDR1_DQSN[3]	DDR0_DQSN[7]
	N30	DDR1_DQSP[3]	DDR0_DQSP[7]
Block 5	AL31	DDR1_DQSN[4]	DDR1_DQSN[2]
	AL30	DDR1_DQSP[4]	DDR1_DQSP[2]
	AU31	DDR1_DQSN[5]	DDR1_DQSN[3]
	AU30	DDR1_DQSP[5]	DDR1_DQSP[3]
Block 7	BC31	DDR1_DQSN[6]	DDR1_DQSN[6]
	BH30	DDR1_DQSP[6]	DDR1_DQSP[6]
	BH31	DDR1_DQSN[7]	DDR1_DQSN[7]
	BH30	DDR1_DQSP[7]	DDR1_DQSP[7]

LOGIC

TABLE

	Pin	DDR3L	LPDDR3	DDR4
Block 1	AF35	DDR1_MA[5]	DDR1_CAA[0]	DDR1_MA[5]
	AB29	DDR1_MA[9]	DDR1_CAA[1]	DDR1_MA[9]
	AE37	DDR1_MA[6]	DDR1_CAA[2]	DDR1_MA[6]
	AE36	DDR1_MA[8]	DDR1_CAA[3]	DDR1_MA[8]
	AC29	DDR1_MA[7]	DDR1_CAA[4]	DDR1_MA[7]
	W29	DDR1_BA[2]	DDR1_CAA[5]	DDR1_BG[0]
	AB28	DDR1_MA[12]	DDR1_CAA[6]	DDR1_MA[12]
	AC28	DDR1_MA[11]	DDR1_CAA[7]	DDR1_MA[11]
Block 3	W28	DDR1_MA[15]	DDR1_CAA[8]	DDR1_ACT#
	Y28	DDR1_MA[14]	DDR1_CAA[9]	DDR1_BG[1]
Block 5	AK35	DDR1_MA[13]	DDR1_CAB[0]	DDR1_MA[13]
	AK34	DDR1_CAS#	DDR1_CAB[1]	DDR1_MA[15]
	AJ35	DDR1_WE#	DDR1_CAB[2]	DDR1_MA[14]
	AJ34	DDR1_RAS#	DDR1_CAB[3]	DDR1_MA[16]
	AJ37	DDR1_BA[0]	DDR1_CAB[4]	DDR1_BA[0]
	AF34	DDR1_MA[2]	DDR1_CAB[5]	DDR1_MA[2]
	AJ36	DDR1_BA[1]	DDR1_CAB[6]	DDR1_BA[1]
	AG34	DDR1_MA[10]	DDR1_CAB[7]	DDR1_MA[10]
	AG35	DDR1_MA[11]	DDR1_CAB[8]	DDR1_MA[11]
	AG36	DDR1_MA[0]	DDR1_CAB[9]	DDR1_MA[0]
	AG37	DDR1_MA[3]	Not Used	DDR1_MA[3]
	AE35	DDR1_MA[4]	Not Used	DDR1_MA[4]

LOGIC

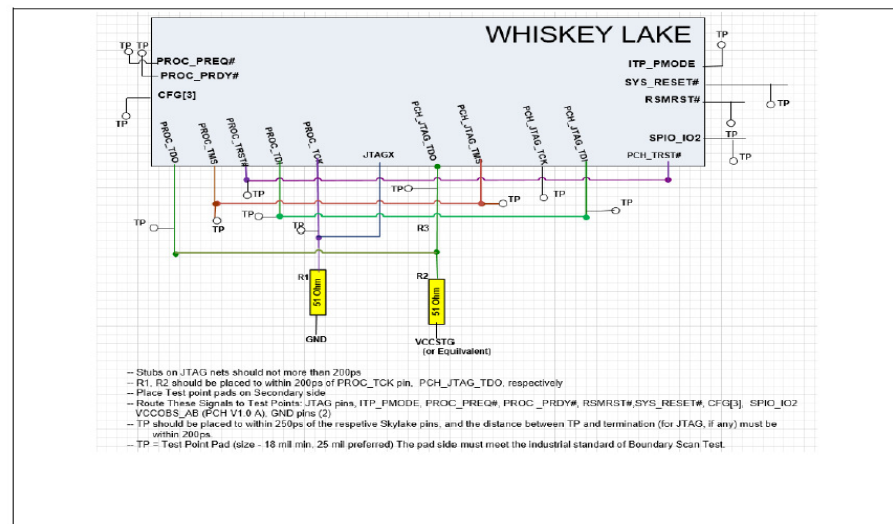
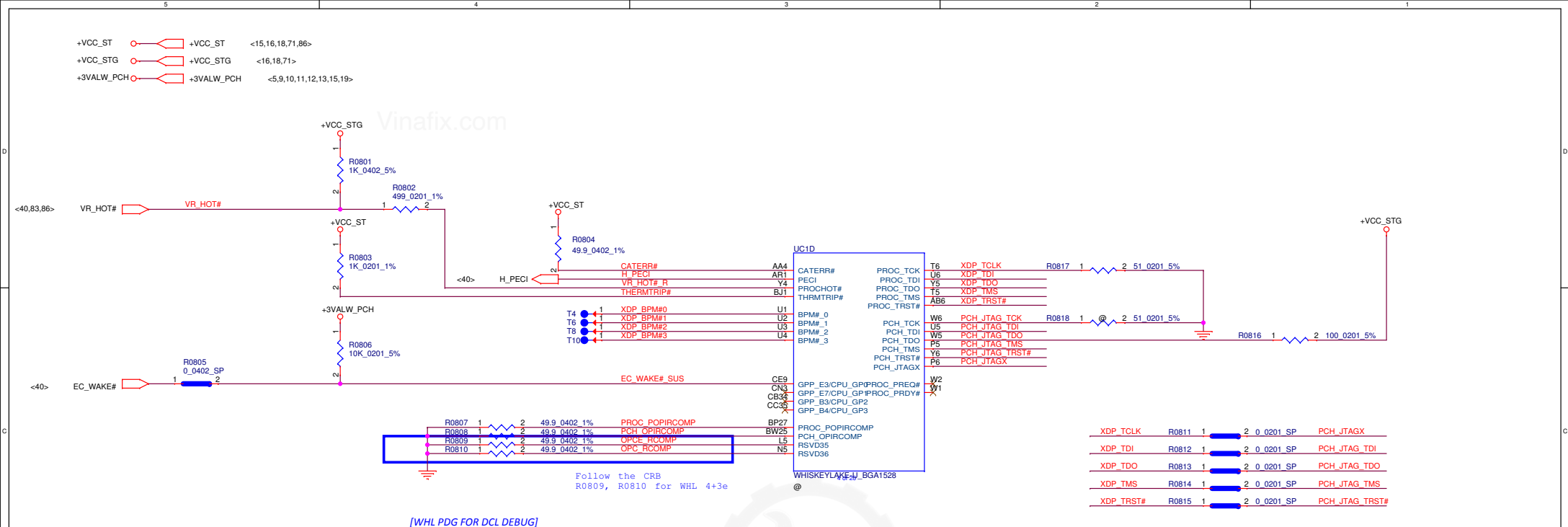
Table 3-1. RCOMP Recommendation for WHL and CFL

Interface	Pin Name	Board Rterm (Ohm)	Board Rdc (Ohm)	Note
DDR - LP3	DDR_RCOMP[0]	200Ω ±1% on pkg to VSS	N/A	
	DDR_RCOMP[1]	80.6Ω ±1% on pkg to VSS	N/A	
	DDR_RCOMP[2]	1620 ±1% on pkg to VSS	N/A	
	DDR_RCOMP[3]	121Ω ±1% on pkg to VSS	N/A	Different RCOMP value in CNL Refer to Table 3-2
DDR - DDR4 SODIMM	DDR_RCOMP[0]	100Ω ±1% on pkg to VSS	N/A	
	DDR_RCOMP[1]	80.6Ω ±1% on pkg to VSS	N/A	
	DDR_RCOMP[2]	100Ω ±1% on pkg to VSS	N/A	

Table 3-2. RCOMP Recommendation for CNL

Interface	Pin Name	Board Rterm (Ohm)	Board Rdc (Ohm)	Note
DDR - DDR4 SODIMM	DDR_RCOMP[0]	100Ω ±1% on pkg to VSS	N/A	No LP3 support in CNL
	DDR_RCOMP[1]	100Ω ±1% on pkg to VSS	N/A	
	DDR_RCOMP[2]	100Ω ±1% on pkg to VSS	N/A	

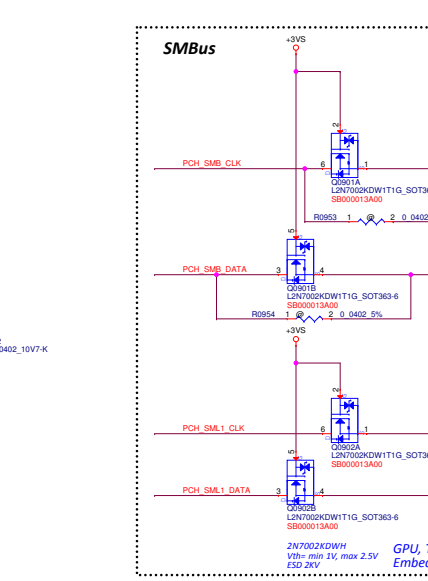
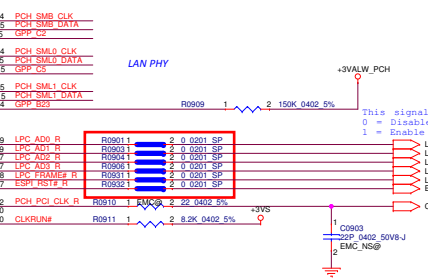
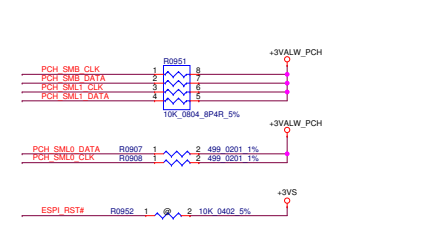
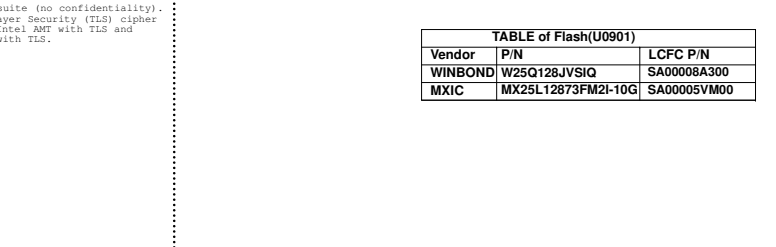
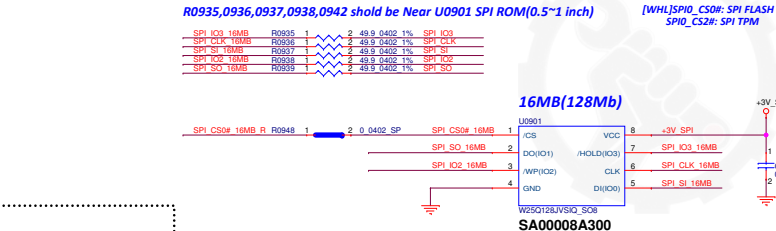
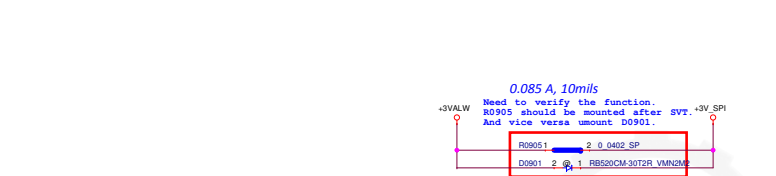
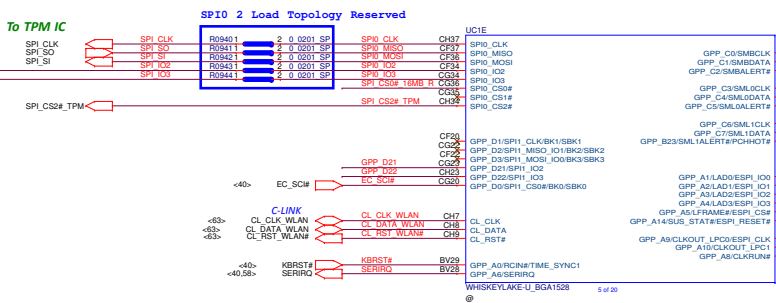
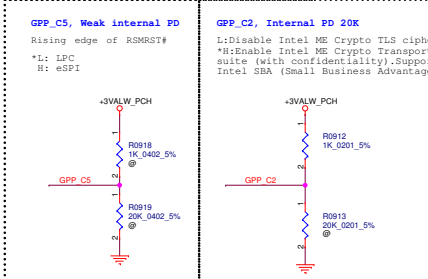
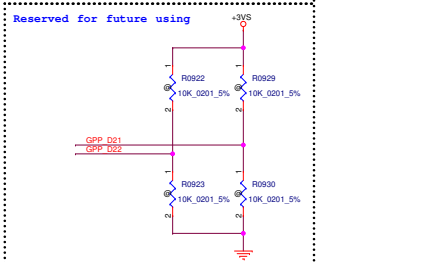
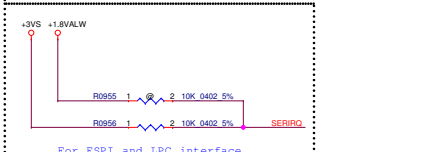
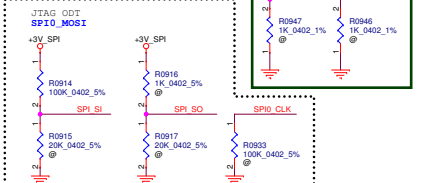
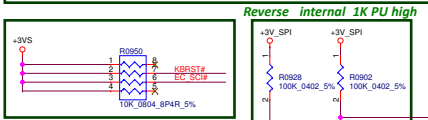
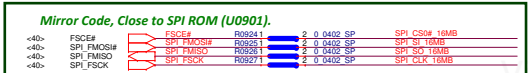
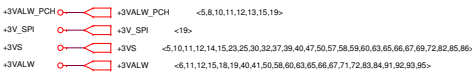




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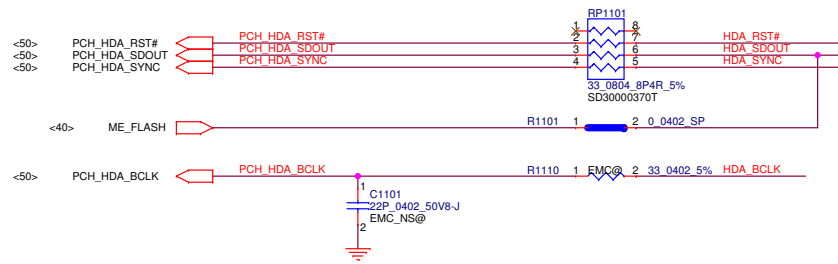


SPI0_MOSI	Reserved	Rising edge of RSMRST#	External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.
SPI0_IO2	Reserved	Rising edge of RSMRST#	External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.
SPI0_IO3	Reserved	Rising edge of RSMRST#	External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.

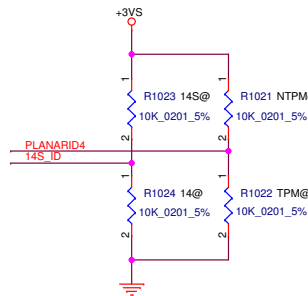
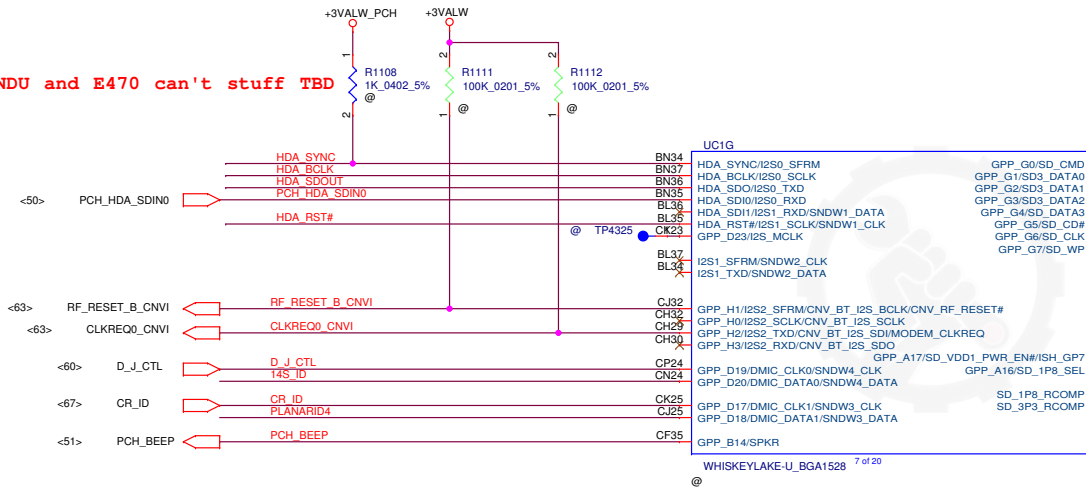
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+3VALW\_PCH <5,8,9,10,12,13,15,19>  
+3VS <5,9,10,12,14,15,23,25,30,32,37,39,40,47,50,57,58,59,60,63,65,66,67,69,72,82,85,86>  
+VCC\_HDA <19>  
+VCC\_IO <5,18,21,71>  
+3VALW <6,9,12,15,18,19,40,41,50,58,60,63,65,66,67,71,72,83,84,91,92,93,95>



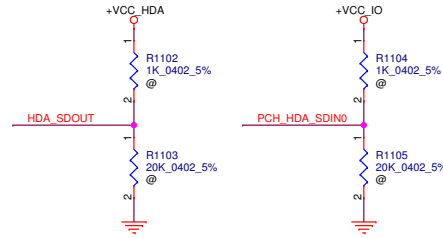
WINDU and E470 can't stuff TBD



Panel ID (Pin#7 Control)		TPM ID	
Status	D_J_CTL (GPP_D19)	Status	PLANARID4 (GPP_D18)
15"	0 (GND Low)	TPM	0 (R1022)
14"	1 (NC High)	NTPM	1 (R1021)

14S ID		Card Reader ID (I/O Board Control)	
Status	14S_ID (GPP_D20)	Status	CR_ID (GPP_D17)
14"	0 (R1024)	CRG	0
14"S	1 (R1023)	CRR	1

To enable Flash Descriptor Security Override, this signal should be pulled up to VCC\_HDA through a 1 KΩ to 2.2 KΩ ± 5% resistor.



GPP\_B14, Internal PD 20K  
No Reboot on TCO  
Timer expiration  
pull-up to VCC3\_3 through a 1~8.2KΩ resistor to disable this capability

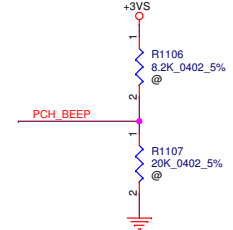
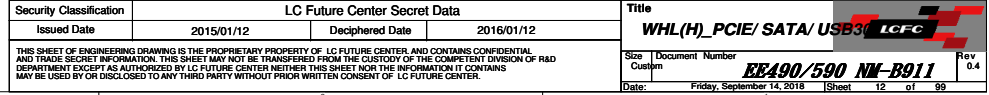


Table 3-1.RCOMP Recommendation for WHL and CFL

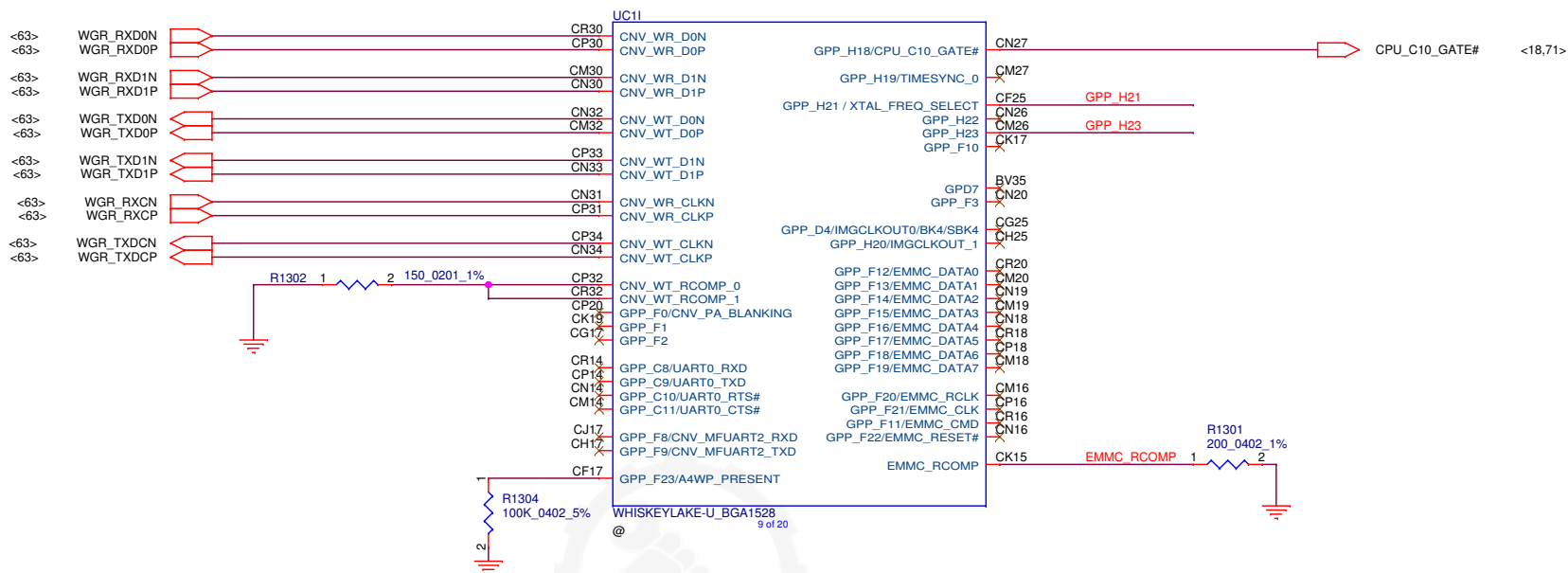
SD3 & EMMC	SD_1P8_RCOMP SD_3P3_RCOMP EMMC_RCOMP	200Ω ±1% to GND	<0.1	Notes: These pins can be merged into one 200Ω +/-1% to GND resistor. Routing each of them to individual 200Ω +/-1% to GND resistor is an option too.



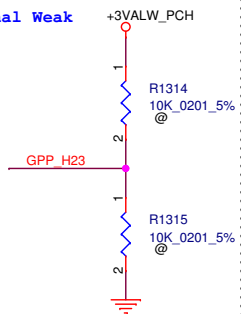
HSIO Configuration	CS19 E14/E15
PCI# 1	Media Card Controller
PCI# 2	Type-A Port
USB3.3	Type-A Port-Gen1(AOU)
USB3.4	Type-A Port-Gen2(DCI)
PCI# 5 x4_L0	dGPU
PCI# 5 x4_L1	dGPU
PCI# 5 x4_L2	dGPU
PCI# 5 x4_L3	dGPU
PCI# 6	GNE PHY
PCI# 7	(Reserved)
PCI# 11	(Reserved)
SATA 1	2.5 HDD
PCI# 13	(Reserved)
PCI# 14	(Reserved)
PCI# 15 x2_L0	PCIe Optane
PCI# 15 x2_L1	PCIe Optane / SATA

+3VS <5,9,10,11,12,14,15,23,25,30,32,37,39,40,47,50,57,58,59,60,63,65,66,67,69,72,82,85,86>  
+3VALW\_PCH <5,8,9,10,11,12,15,19>

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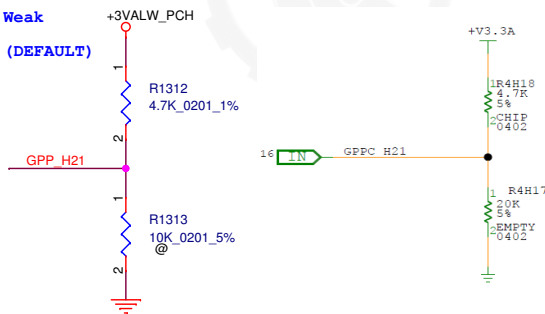



GPP\_H23, Internal Weak pull-down



This strap must be configured to 0 (SAFS is disabled) if the eSPI or LPC strap is configured to 0 (eSPI is disabled)

GPP\_H21, Internal Weak pull-down  
LOW: 38.4/19.2MHZ (DEFAULT)  
HIGH: 24MHZ

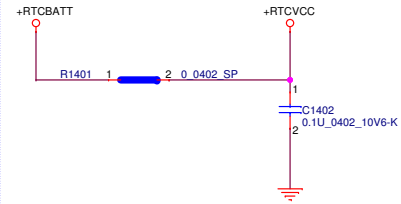


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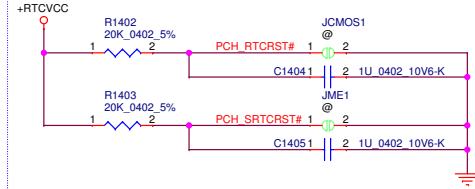
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+RTCVCC <15,19>  
+3VS <5,9,10,11,12,15,23,25,30,32,37,39,40,47,50,57,58,59,60,63,65,66,67,69,72,82,85,86>

#### RTC External Circuit

+RTCBATT, +RTCVCC  
Trace width = 20mils

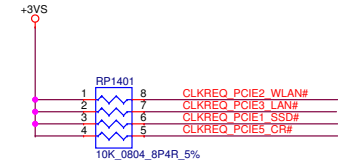
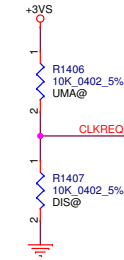
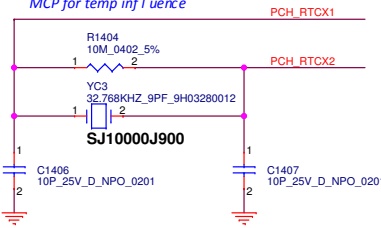


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#### RTC Crystal

1. Space > 15mils
2. No trace under crystal
3. Place on opposit side of MCP for temp influence



#### HDD

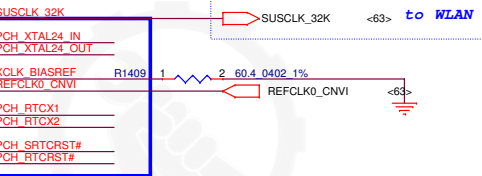
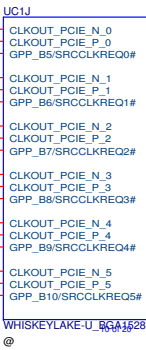
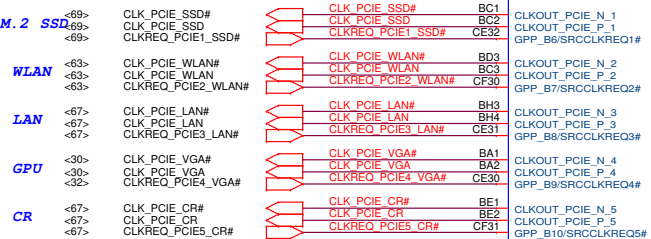
#### M.2 SSD

#### WLAN

#### LAN

#### GPU

#### CR



#### Need close CPU

#### EMC

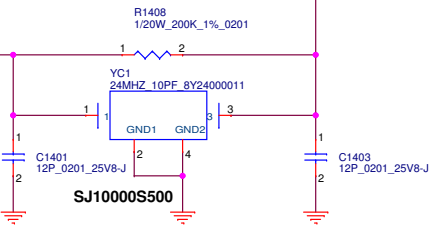
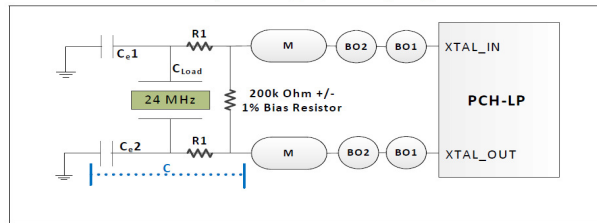
#### FOOTPRINT:R\_0402

#### EMC

#### FOOTPRINT:R\_0402

#### 7.3.2.3 WHLU PCH-LP Platform XTAL Routing Guidelines

Figure 7-7. WHLU PCH-LP Platform Crystal XTAL\_IN/OUT Topology

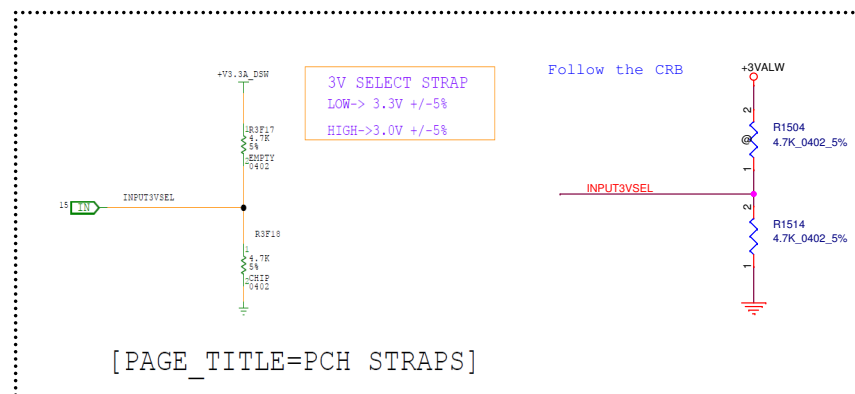
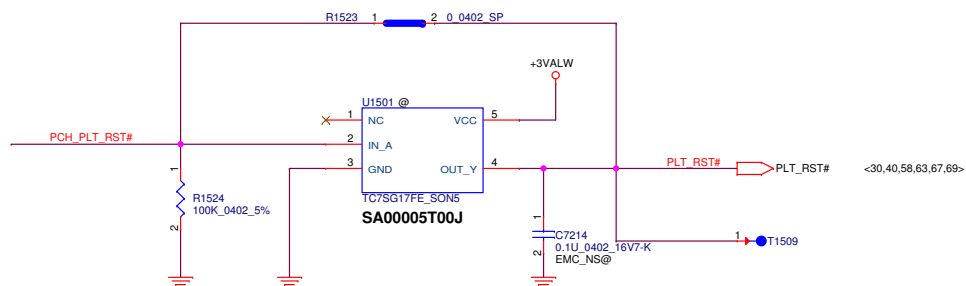
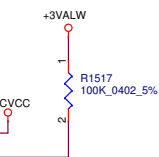
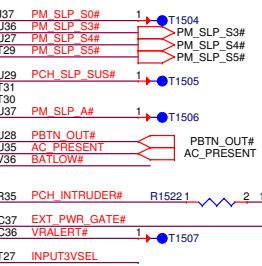
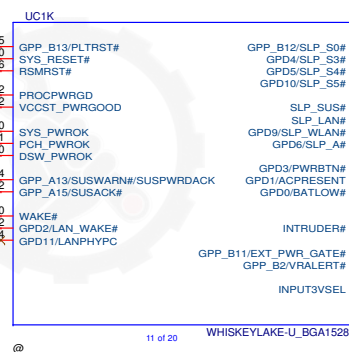
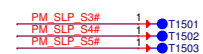
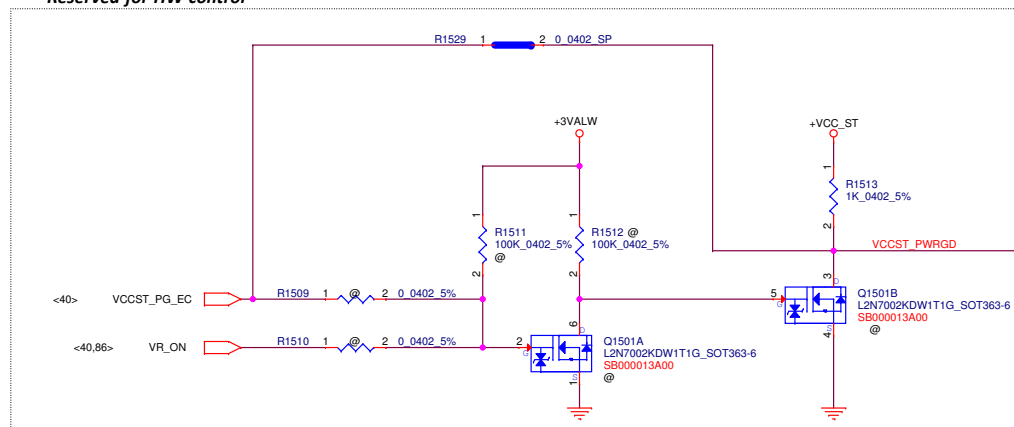
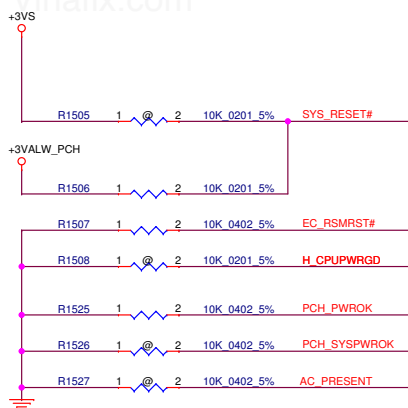



YC1  
Equivalent resistance (RR) = 30 Ohm

TABLE of XTAL (YC1)		
Vendor	P/N	LCFC P/N
TXC	8Y24000034	SJ10000S500
HARMONY	X2C024000DC1H-HU	SJ10000RR00

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+VCC\_GT <27,88,90>  
+VCC\_CORE <16,27,87,90>  
+VCCCPUCORE\_GT <27>

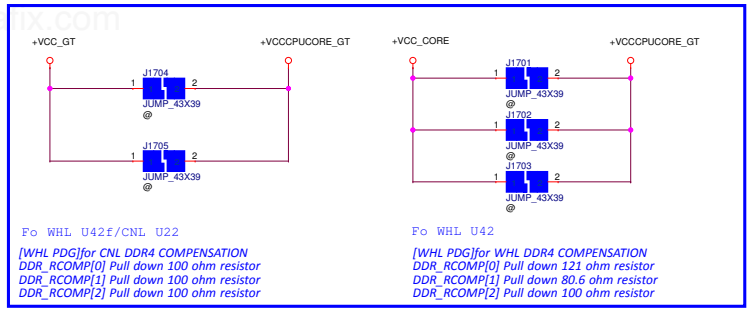


Figure 11-11.Whiskey Lake U 4+2/Coffee Lake U 4+2f/Cannon Lake U 2+2/Coffee Lake U 4+3e Processor - RSHUNT Routing and Placement Guideline

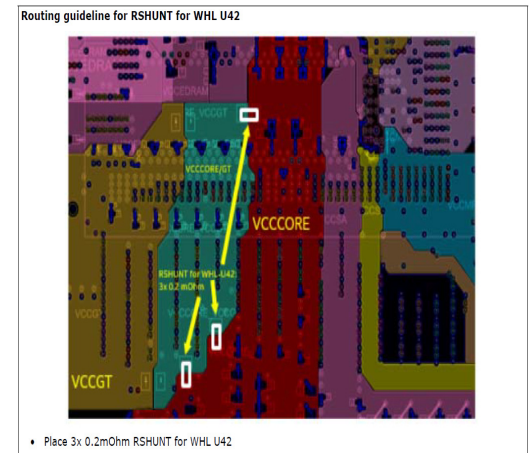
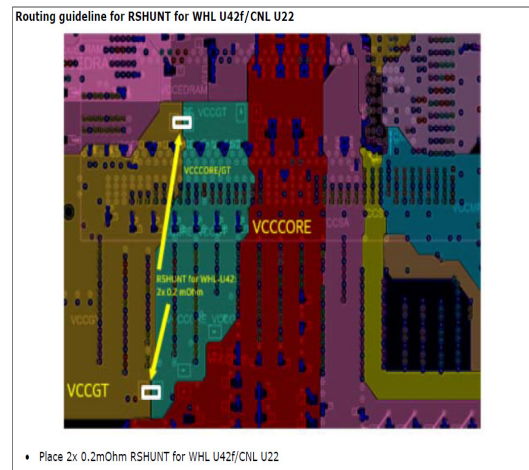
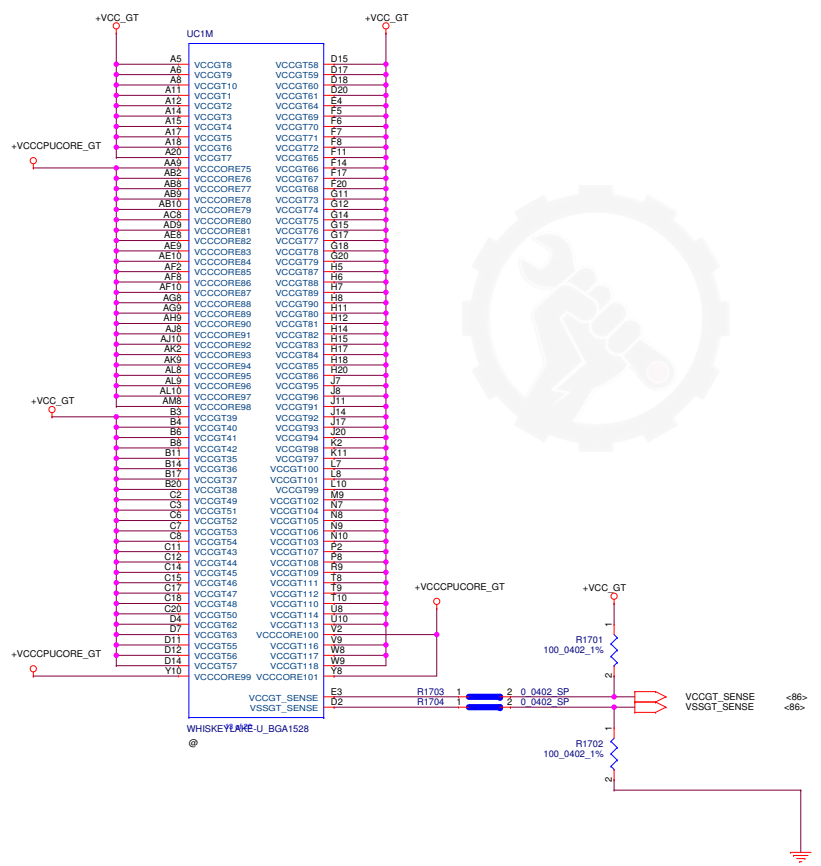


Figure 11-11.Whiskey Lake U 4+2/Coffee Lake U 4+2f/Cannon Lake U 2+2/Coffee Lake U 4+3e Processor - RSHUNT Routing and Placement Guideline



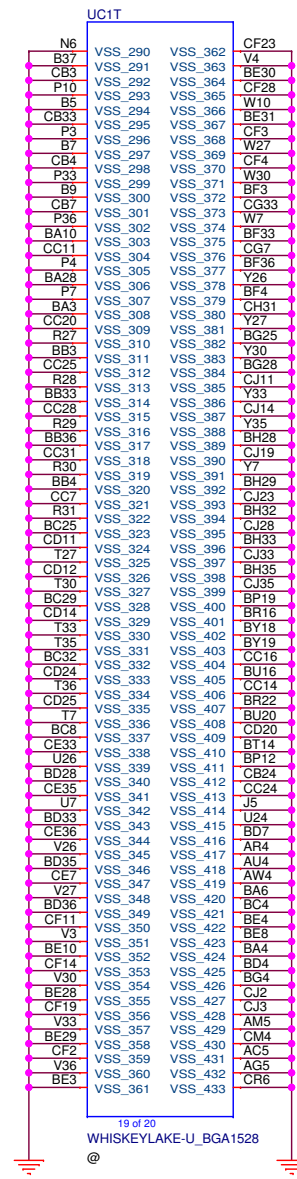
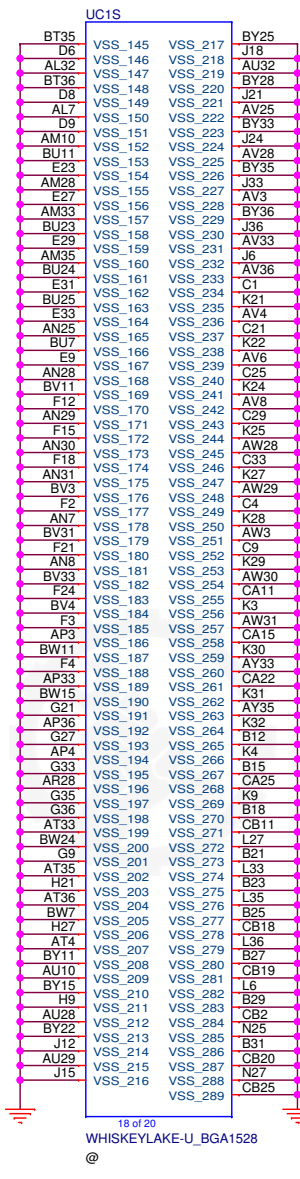
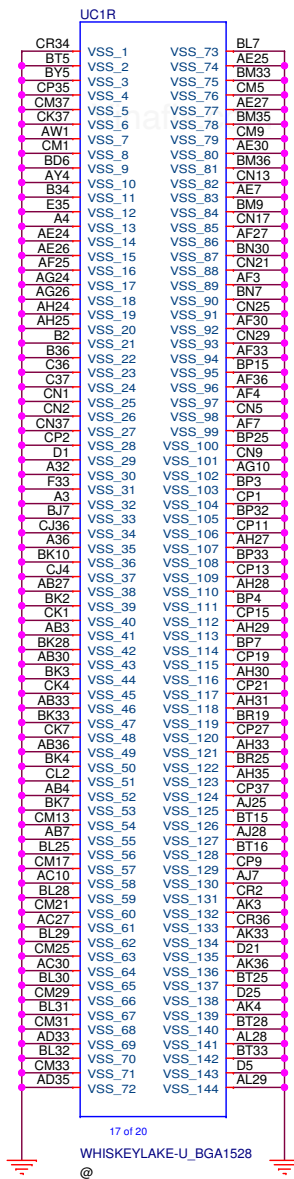
575414 WHL\_Ballout List

Pin Number	CFL U42e	WHL U42 QS/Production	CNL U22/WHL-U42 ESO/1
AA9	VCCGT	VCCCORE	VCCGT
AB10	VCCGT	VCCCORE	VCCGT
AB2	VCCGT	VCCCORE	VCCGT
AB8	VCCGT	VCCCORE	VCCGT
AB9	VCCGT	VCCCORE	VCCGT
AC3	VCCGT	VCCCORE	VCCGT
AD9	VCCGT	VCCCORE	VCCGT
AE10	VCCGT	VCCCORE	VCCGT
AE8	VCCGT	VCCCORE	VCCGT
AE9	VCCGT	VCCCORE	VCCGT
AF10	VCCGT	VCCCORE	VCCGT
AF2	VCCGT	VCCCORE	VCCGT
AF8	VCCGT	VCCCORE	VCCGT
AG8	VCCGT	VCCCORE	VCCGT
AG9	VCCGT	VCCCORE	VCCGT
AH9	VCCGT	VCCCORE	VCCGT
AI10	VCCGT	VCCCORE	VCCGT
AJ8	VCCGT	VCCCORE	VCCGT
AK2	VCCGT	VCCCORE	VCCGT
AK9	VCCGT	VCCCORE	VCCGT
AL10	VCCGT	VCCCORE	VCCGT
AL8	VCCGT	VCCCORE	VCCGT
AL9	VCCGT	VCCCORE	VCCGT
AM8	VCCGT	VCCCORE	VCCGT
V2	VCCGT	VCCCORE	VCCGT
Y10	VCCGT	VCCCORE	VCCGT
Y8	VCCGT	VCCCORE	VCCGT



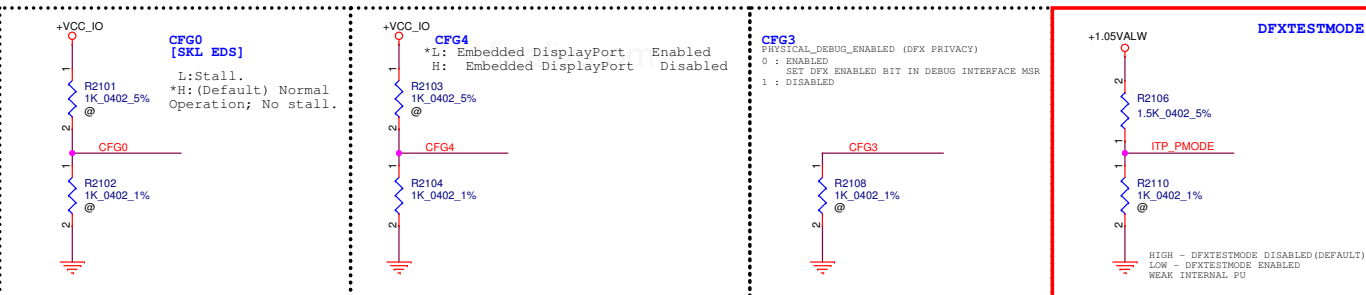






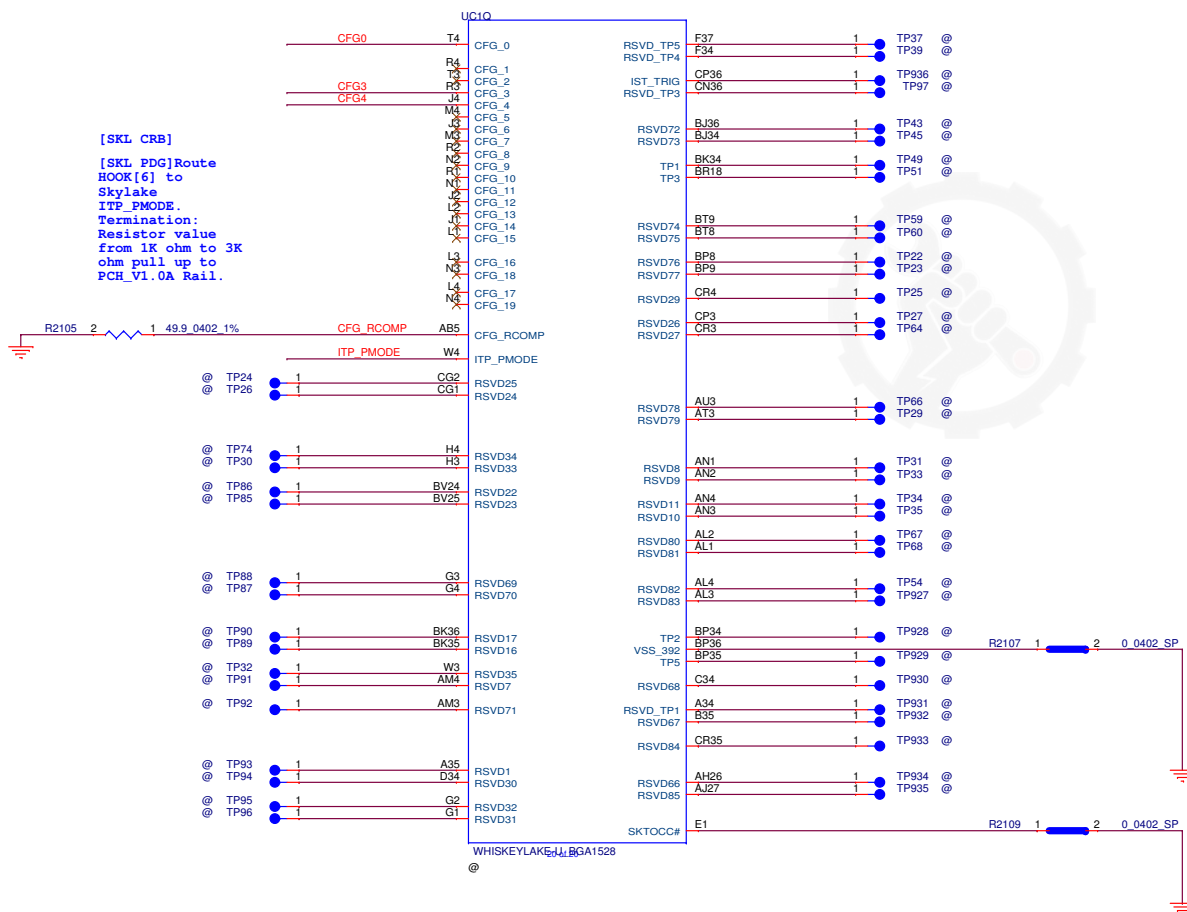
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+1.05VALW <19,71,92>  
+VCC\_IO <5,11,18,71>



20180528  
Change the Netname to +1.05VALW  
Modified By Tony

[SKL CRB]  
[SKL PDG]Route  
HOOK[6] to  
Skylake  
ITP\_PMODE.  
Termination:  
Resistor value  
from 1K ohm to 3K  
ohm pull up to  
PCH\_V1.0A Rail.



TABLE

**CFG0 : Stall Reset Sequence**  
after PCU PLL Lock until de-asserted  
1 : No Stall  
0 : Stall

**CFG4 : eDP Enable**  
1 : Disabled  
0 : Enabled

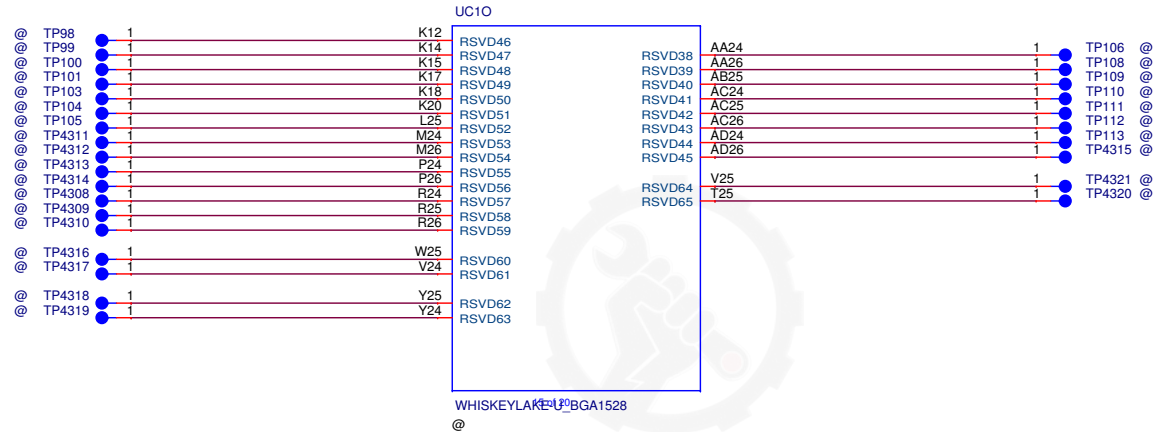
**CFG9 : SVID Bus Communication**  
1 : Enabled  
0 : Disabled


[SKL EDS]Zero Voltage Mode:VCCOPC is fixed OPC VR output voltage of 1V, the processor can drive VR to LPM (Low Power Mode) which sets VR output to 0V using ZVM# signal as shown below:

ZVM#	state	VCCOPC
0V		0V
1V		1V

[SKL EDS]Minimum Speed Mode: VCCEPIO can be connected to OPC VR in this case VCCEPIO is fixed to 1V. The processor can drive VR to LPM (Low Power Mode) which sets VR output to 0V using ZVM# signal. In order to achieve better power/performance it is recommended to use a separate VR for VCCEPIO in this case VCCEPIO is configurable to 0.8V/1V. The processor drives the VR to set VCCEPIO value(0.8V/1V) using MSM# signal, based on the required bandwidth for the EPIO interface as shown below:

ZVM#	state	MSM#	state	VCCEPIO
0V		X		0V
1V		0V		0.8V
1V		1V		1V

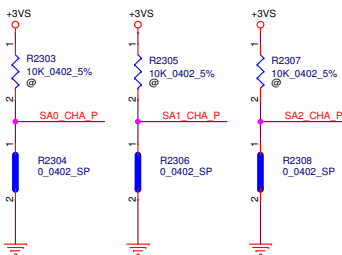
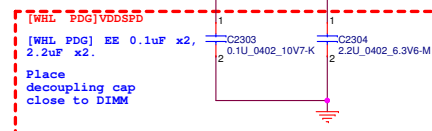
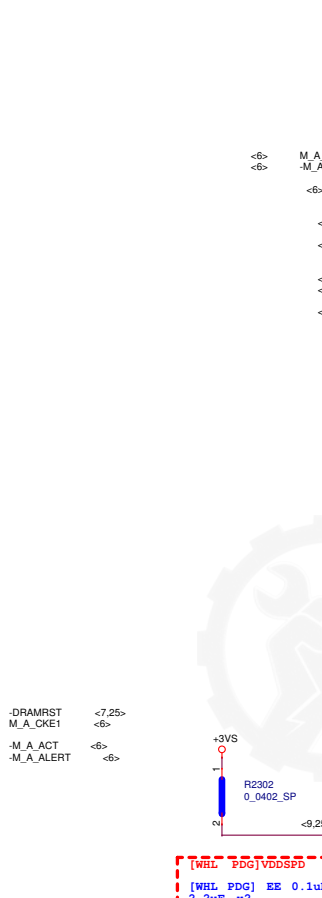


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SPD Address = 0H



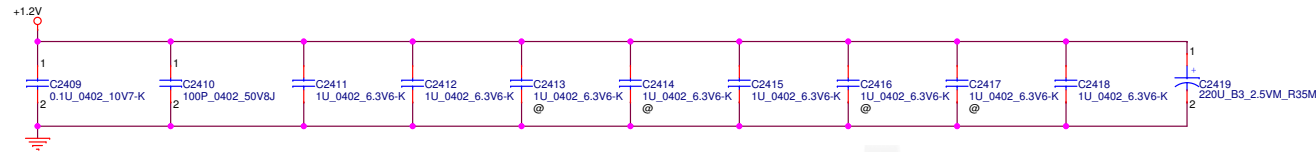
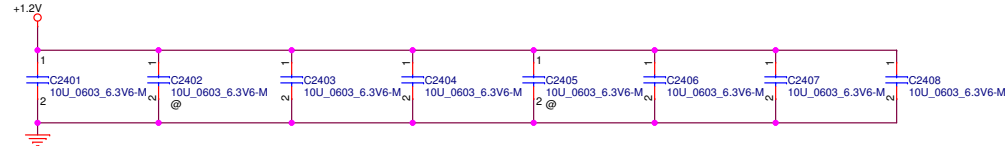
+2.5V  
+1.2V  
+0.6VS

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[WHL PDG]VDDQ  
[WHL PDG] EE 10uF x16, 1uF x16. 330uF x1

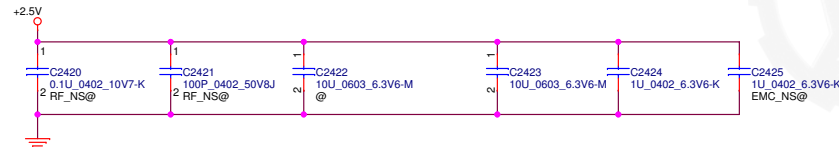
Place 10uF/1uF decoupling cap, 4  
near each side of the DIMM  
connector close to VDD pins.  
330uF placeholder

Total quantity is referring to 2 channels.



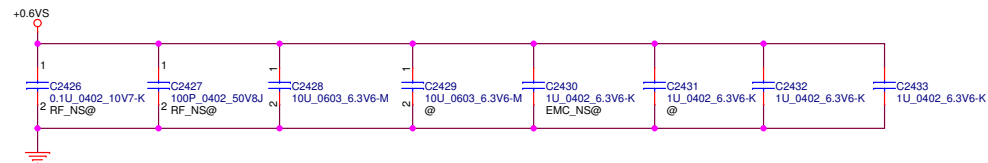
10U x 6  
0.1U x 2  
1U x 4  
220U x 1

[WHL PDG]VPP  
[WHL PDG] EE 10uF x2, 1uF x2.  
Place decoupling cap on DRAM side.



10U x 1  
1U x 1

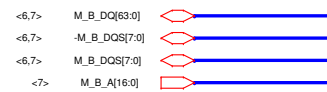
[WHL PDG]VTT  
[WHL PDG] EE 10uF x2, 1uF x4.



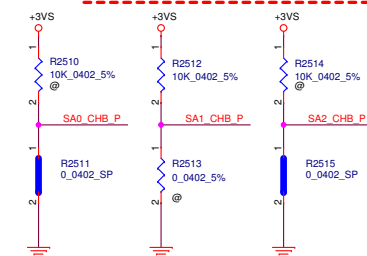
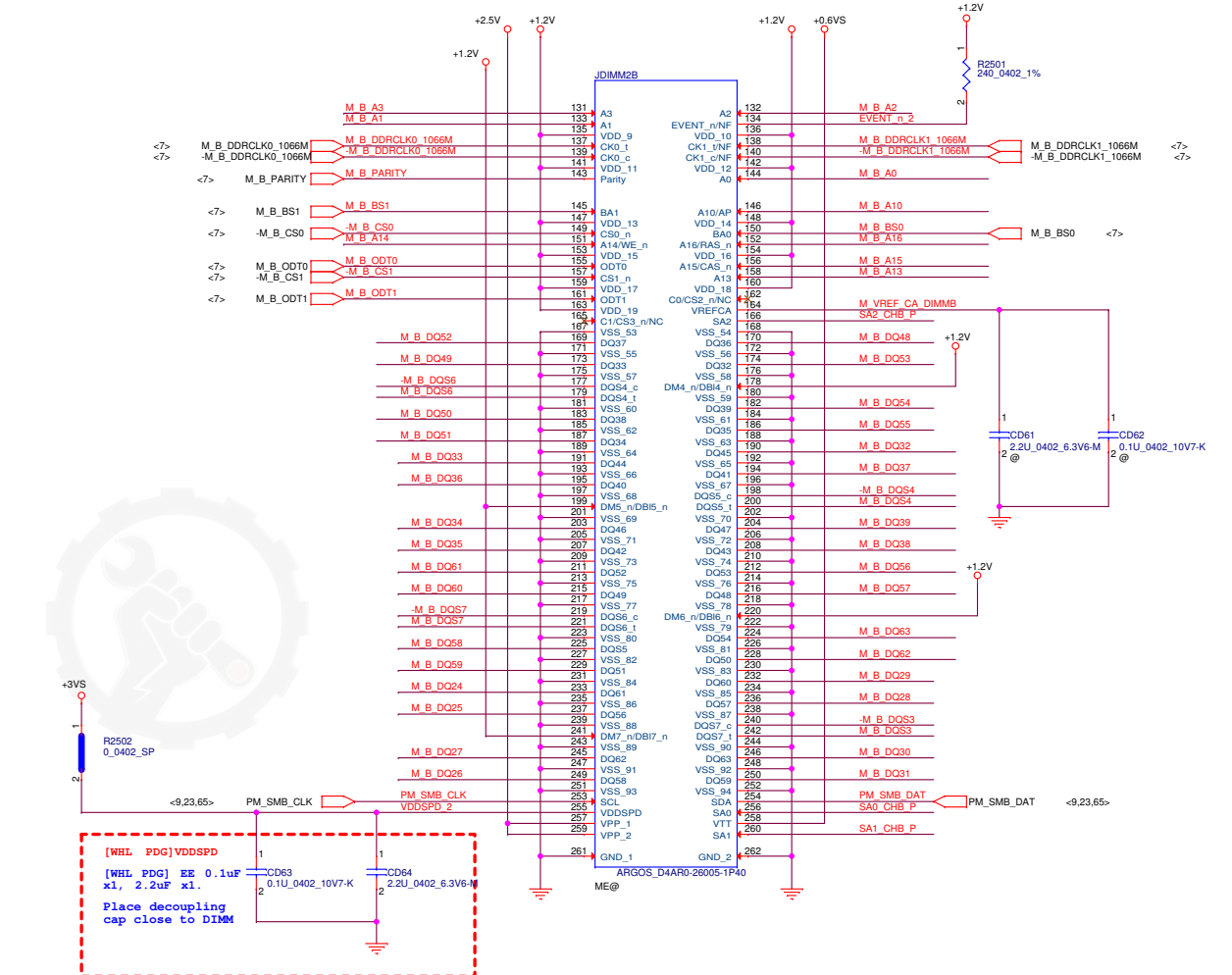
10U x 1  
1U x 2

Place decoupling on the VTT plane close to SODIMM

Total  
10U x 8  
0.1U x 2  
1U x 7  
220U x 1



Layout Node:  
Place Close DIMMs



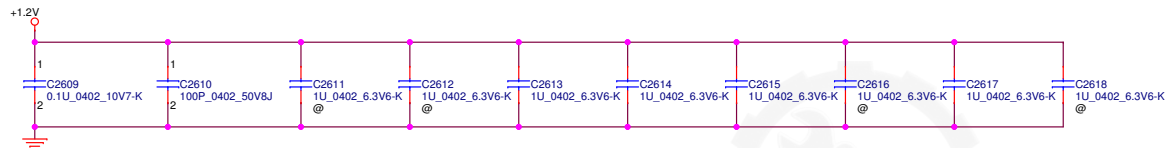
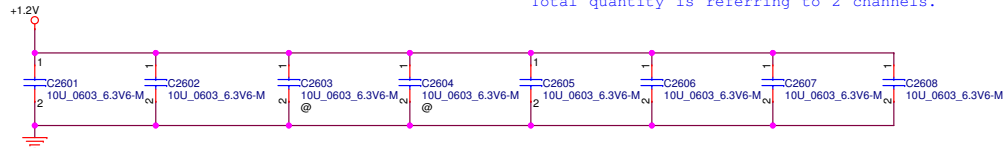
Signal Name	Description	Dir.	Buffer Type	Link Type	Availability
DDR0_DQSP[8:0] DDR0_DQSN[8:0] DDR1_DQSP[8:0] DDR1_DQSN[8:0]	<b>Data Strobes:</b> Differential data strobe pairs. The data is captured at the crossing point of DQS during read and write transactions.	I/O	DDR4/-RS	Diff	The 9th signals[8] are applicable for UDIMM/ SODIM module with ECC in S and H-processor line processors



+2.5V  
+1.2V  
+0.6VS

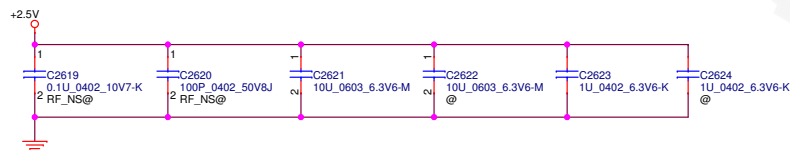
[WHL PDG]VDDQ  
[WHL PDG] EE 10uF x16, 1uF x16. 330uF x1  
Place 10uF/1uF decoupling cap, 4  
near each side of the DIMM  
connector close to VDD pins.  
330uF placeholder

Total quantity is referring to 2 channels.



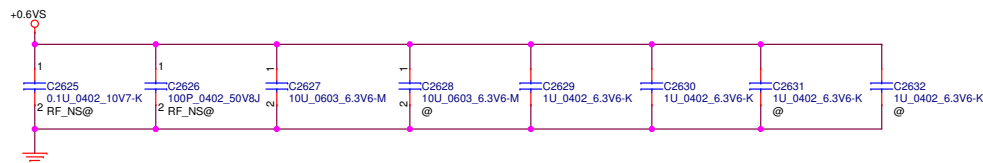
10U x 6  
0.1U x 2  
1U x 4

[WHL PDG]VPP  
[WHL PDG] EE 10uF x2, 1uF x2.  
Place decoupling cap on DRAM side.



10U x 1  
1U x 1

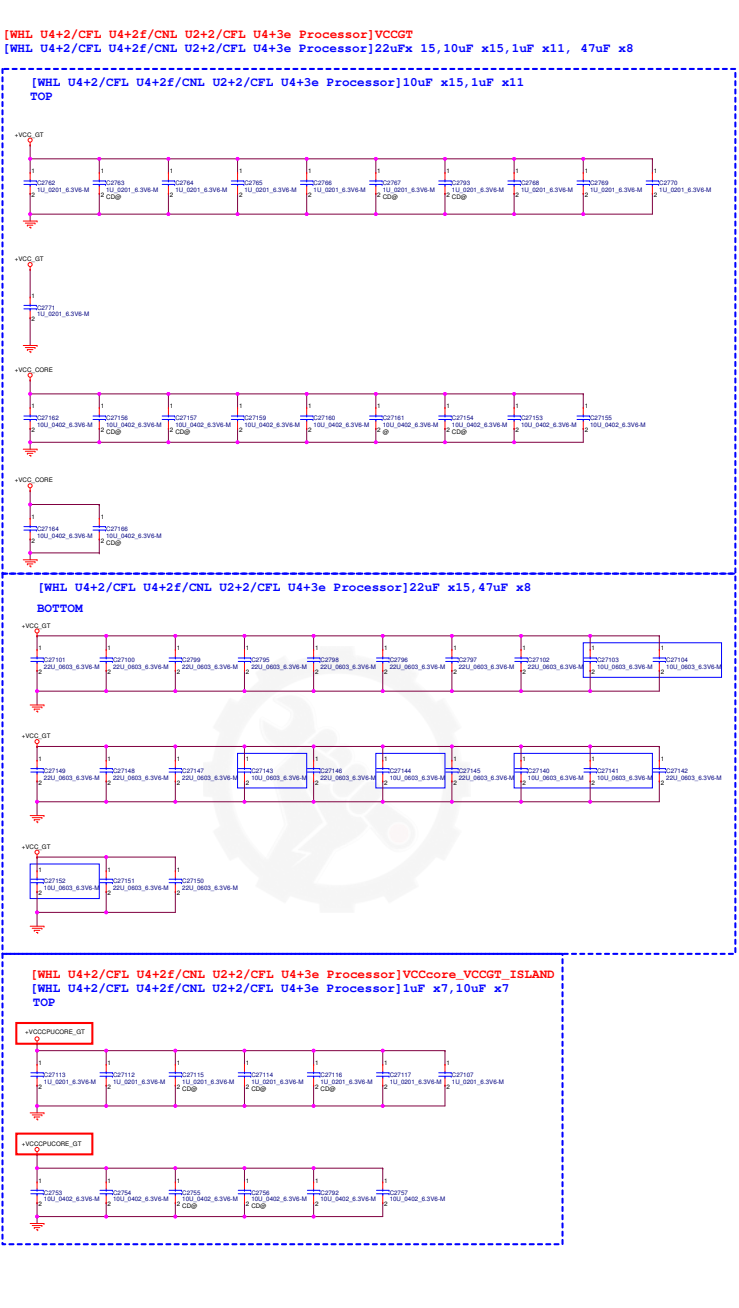
[WHL PDG]VTT  
[WHL PDG] EE 10uF x2, 1uF x4.



10U x 1  
1U x 2


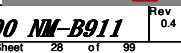
Place decoupling on the VTT plane close to SODIMM

Total  
10U x 8  
0.1U x 2  
1U x 7



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				Date:	Friday, September 14, 2018	Sheet	28 of 99
						Rev	0.4

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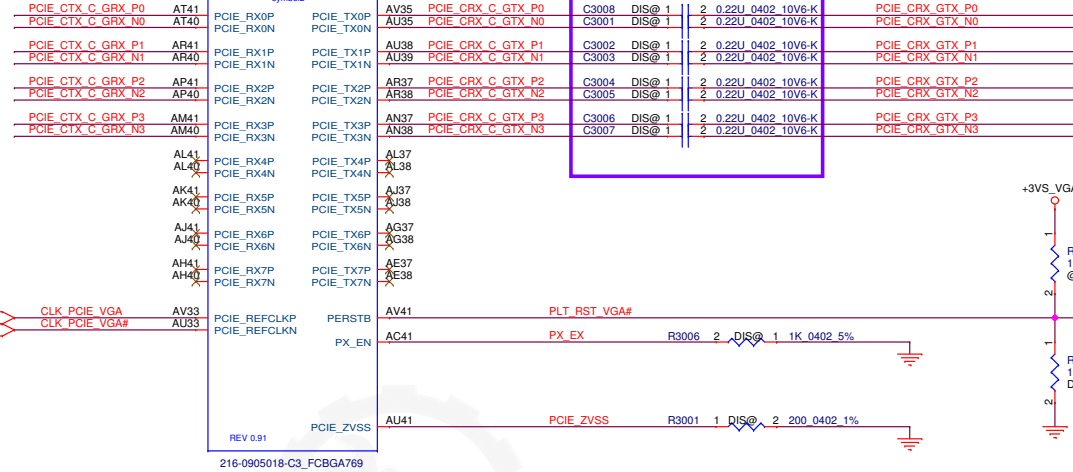
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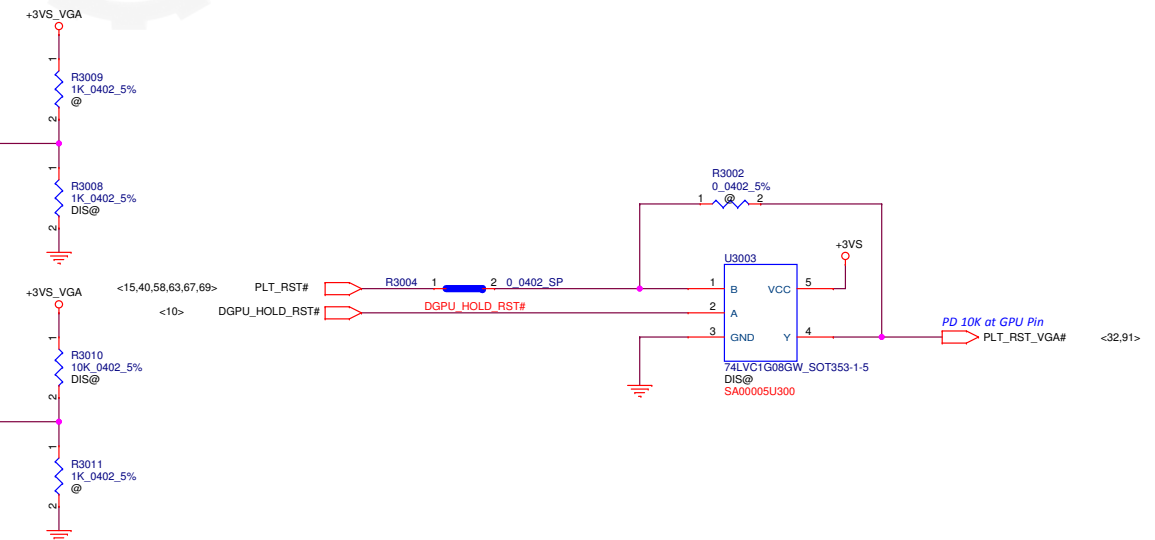
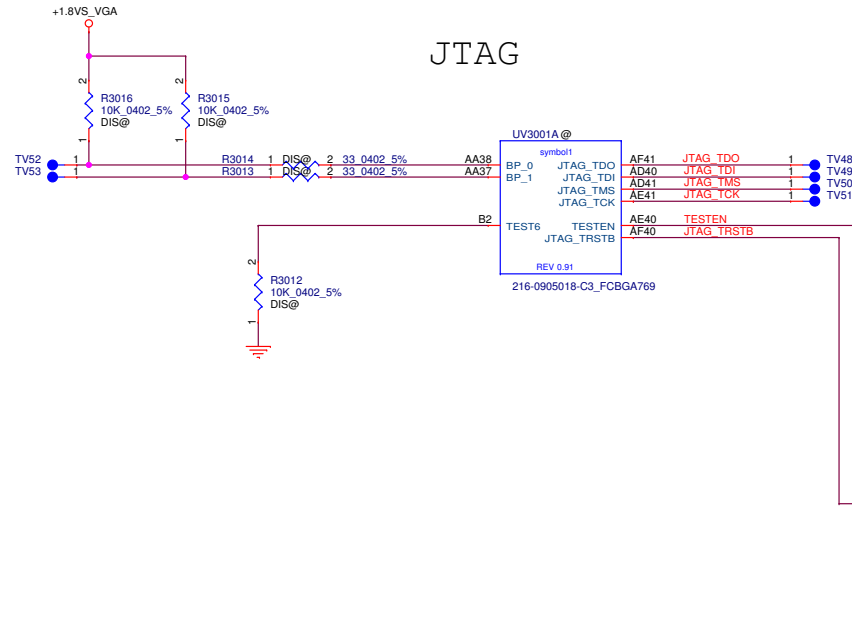


TABLE of GPU (UV3001)		
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AMD(R17M-P1-70)	SA00008ED00	S IC 216-0905004 C0 FCBGA 769P GPU
AMD(R17M-P1-50)	SA00008DT10	S IC 216-0905018 C3 FCBGA 769P GPU

DIS@ support GEN3



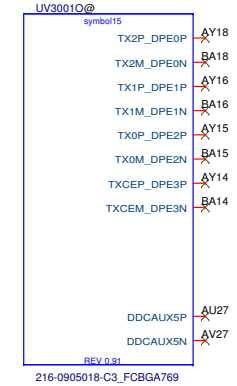
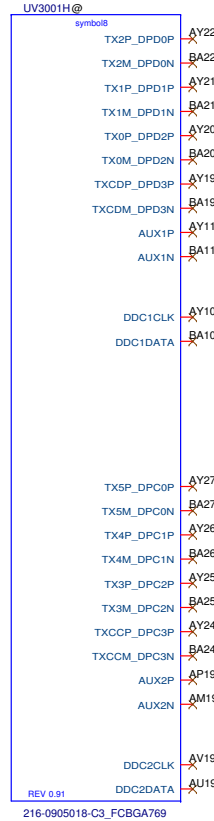
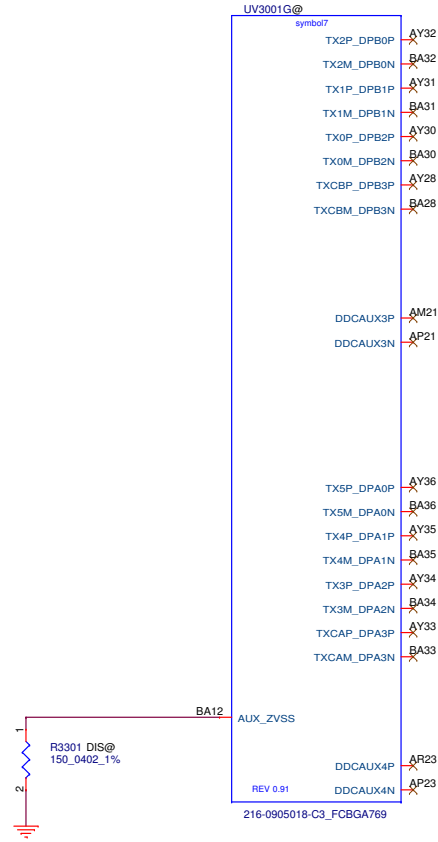
JTAG



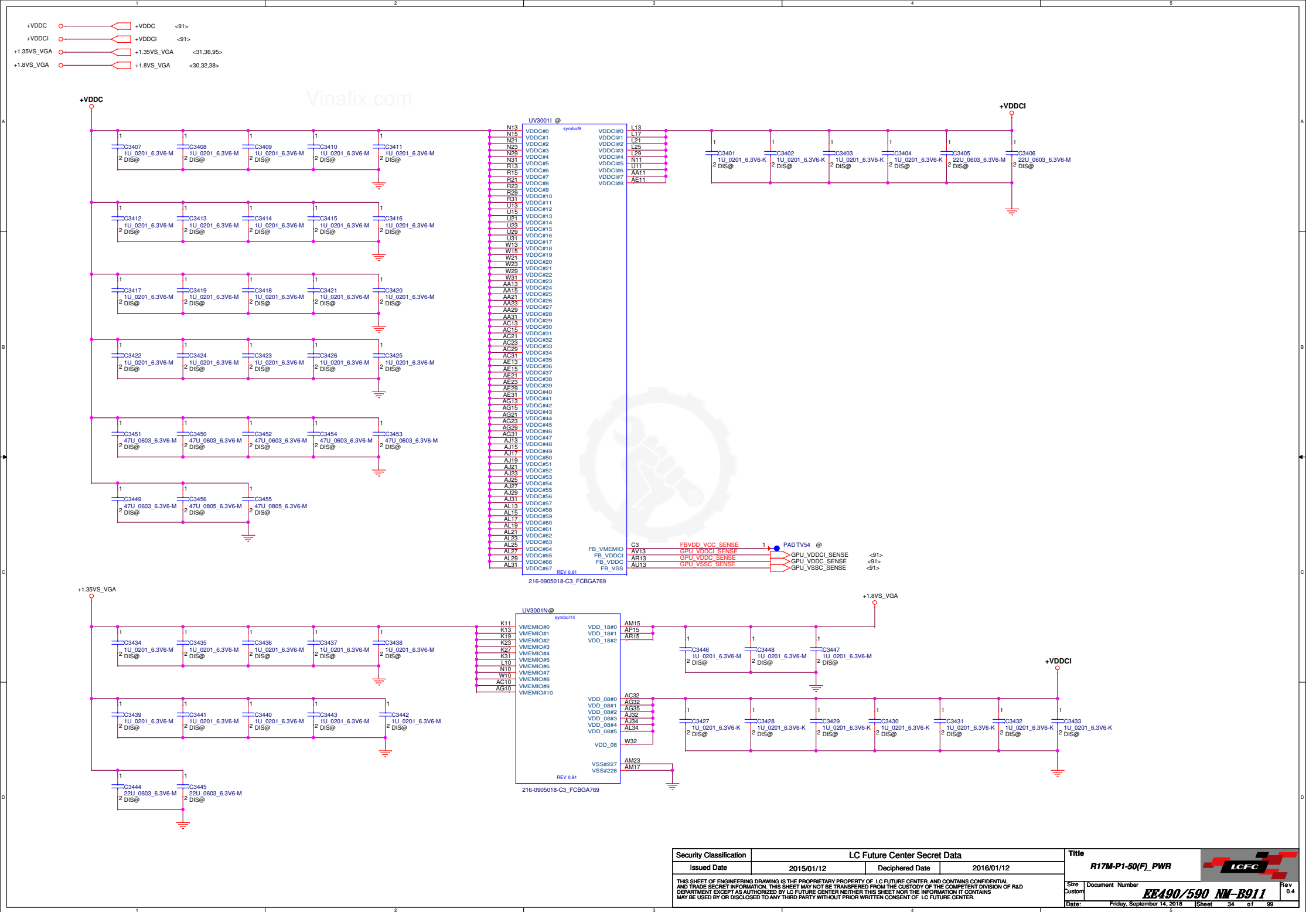
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Issued Date				2015/01/12		Deciphered Date		2016/01/12		Size		Document Number	
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										Sheet		30	
										01		99	

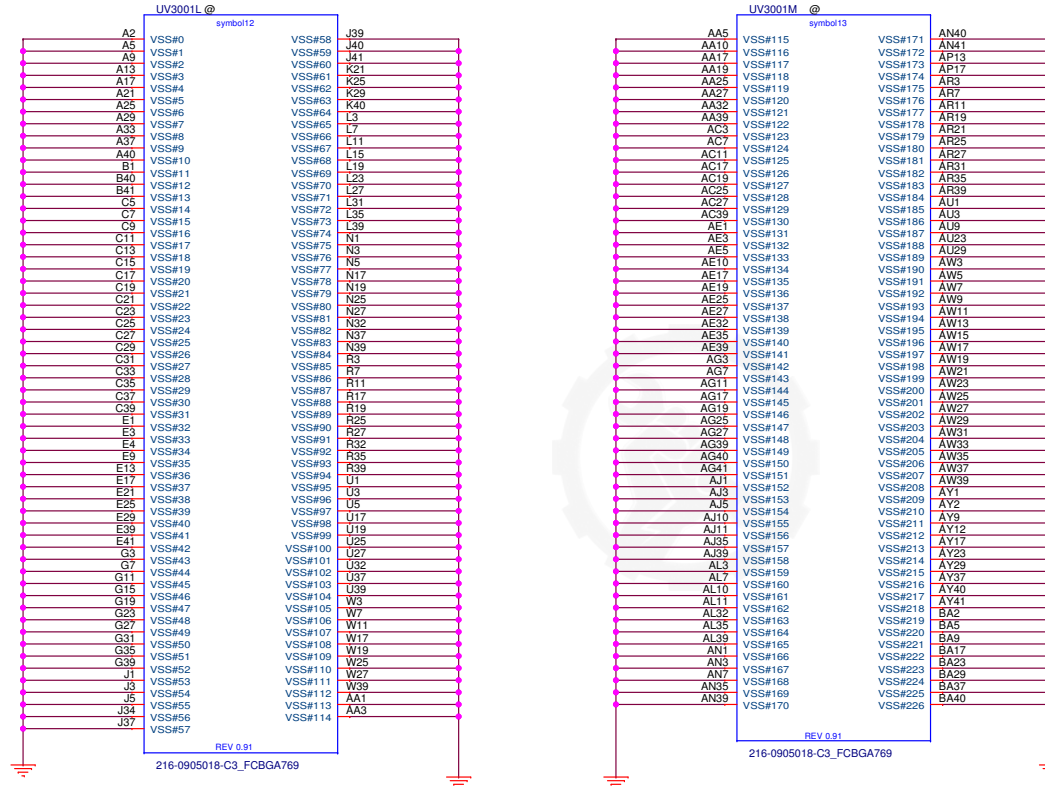






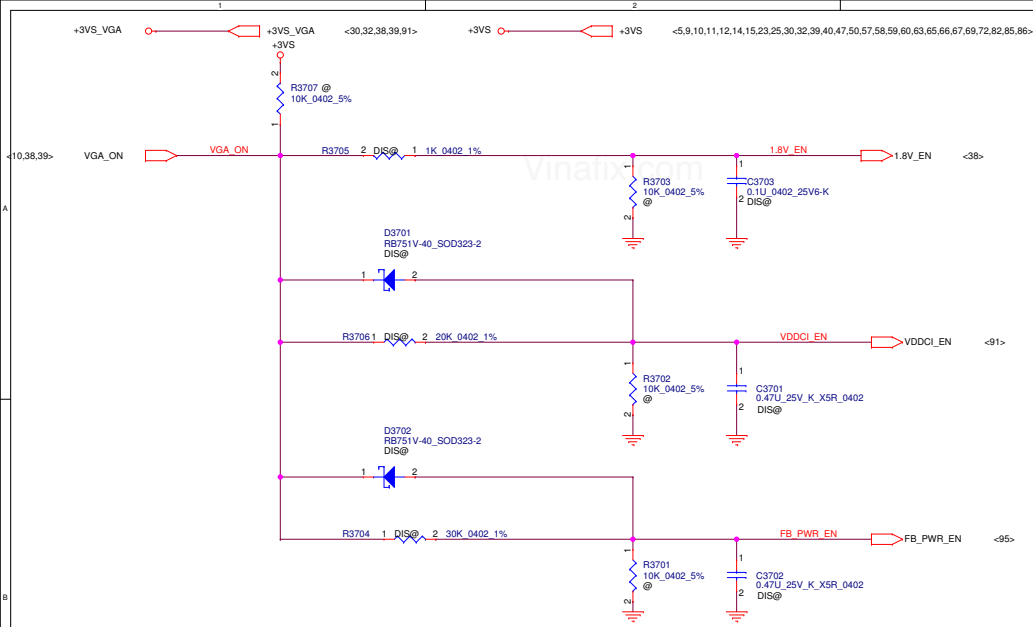
If this interface is not used, all signal outputs can be unconnected. AUX\_ZVSS should always be connected.



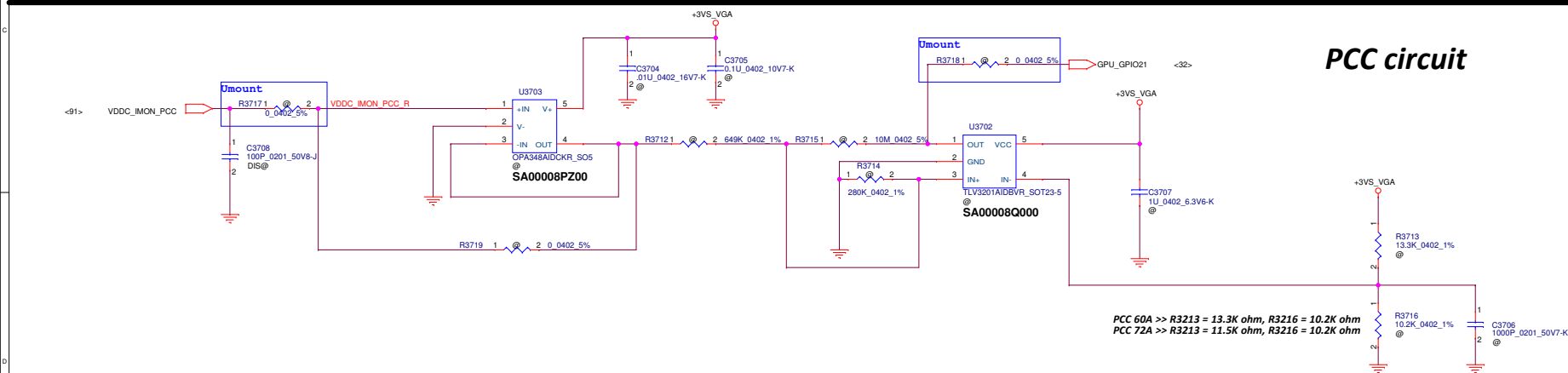
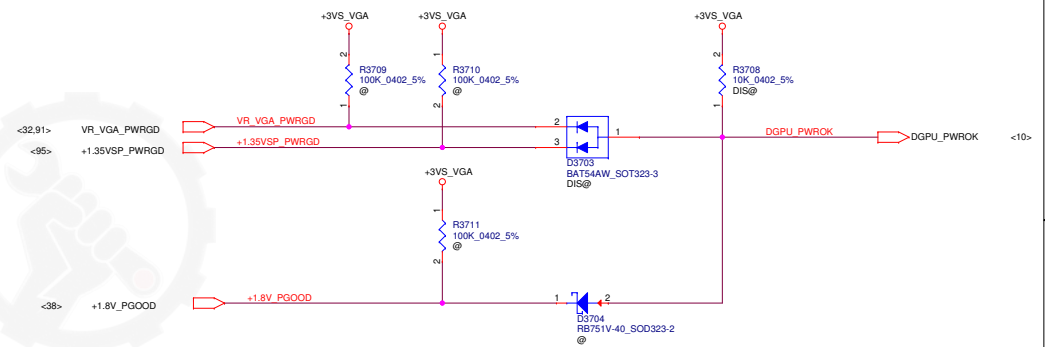
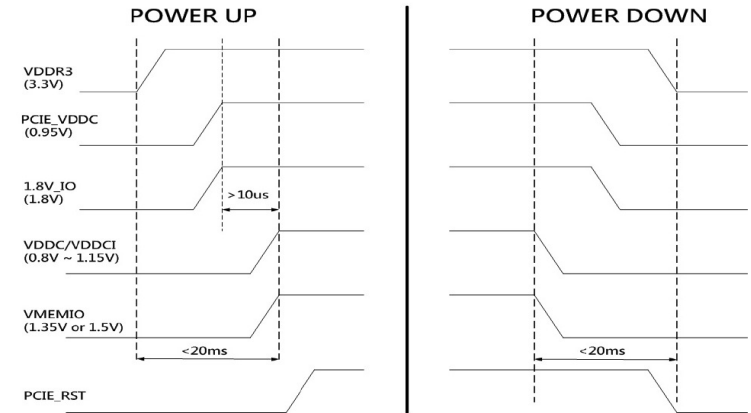








## POWER UP / POWER DOWN SEQUENCE



## PCC circuit

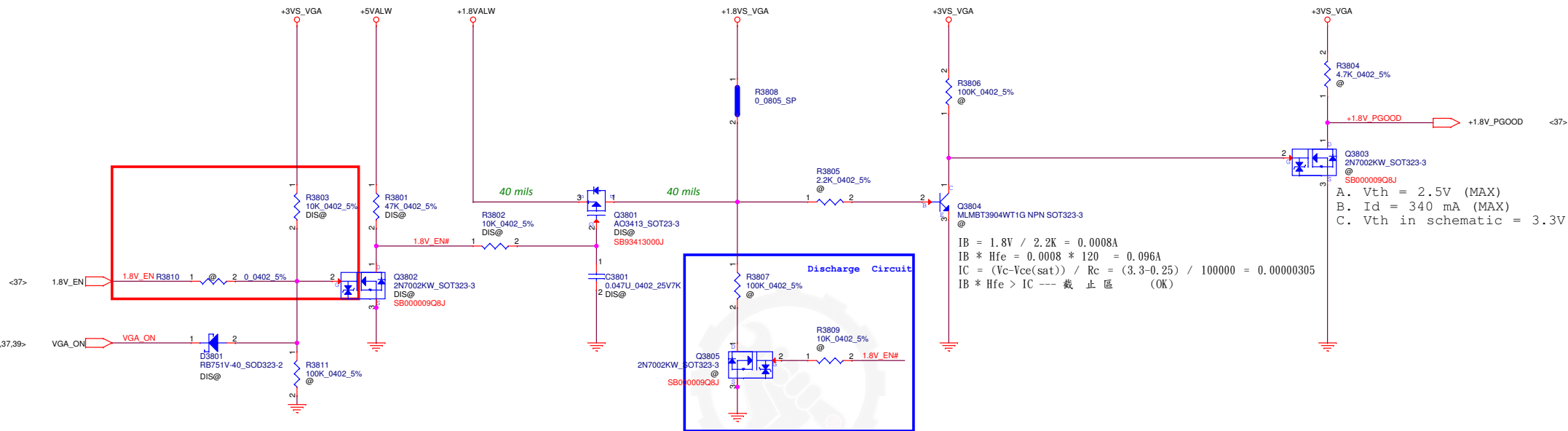
PCC 60A >> R3213 = 13.3K ohm, R3216 = 10.2K ohm  
PCC 72A >> R3213 = 11.5K ohm, R3216 = 10.2K ohm

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+3VS\_VGA <30,32,37,39,91>  
+5VALW <39,41,42,43,47,62,64,66,67,71,72,84,85,86,87,88,89,91,93,94>  
+1.8VALW <9,19,40,50,51,63,93>  
+1.8VS\_VGA <30,32,34>

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## +1.8VALW to +1.8VS\_VGA



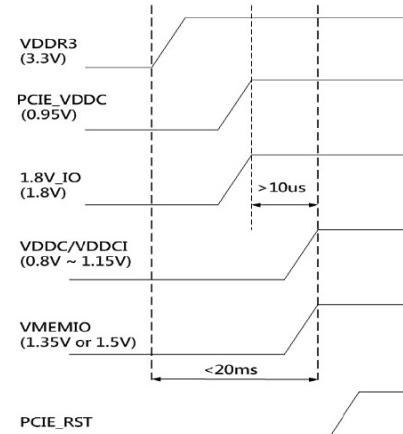
Security Classification	LC Future Center Secret Data			Title
Issued Date	2015/01/12	Deciphered Date	2016/01/12	DC V TO 1.5VS_VGA/1.8VS_VGA
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+3VS\_VGA ○ +3VS\_VGA <30,32,37,38,91>  
 +5VALW ○ +5VALW <38,41,42,43,47,62,64,66,67,71,72,84,85,86,87,88,89,91,93,94>  
 +3VS ○ +3VS <5,9,10,11,12,14,15,23,25,30,32,37,40,47,50,57,58,59,60,63,65,66,67,69,72,82,85,86>

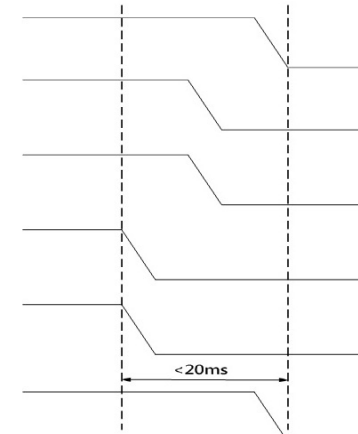
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## POWER UP / POWER DOWN SEQUENCE

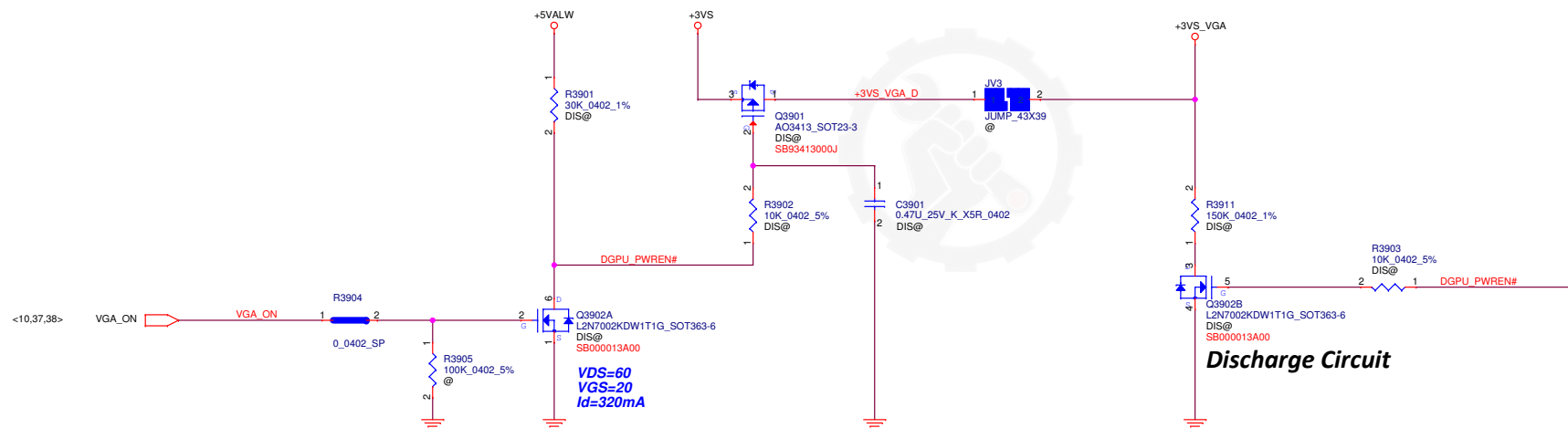
### POWER UP




### POWER DOWN

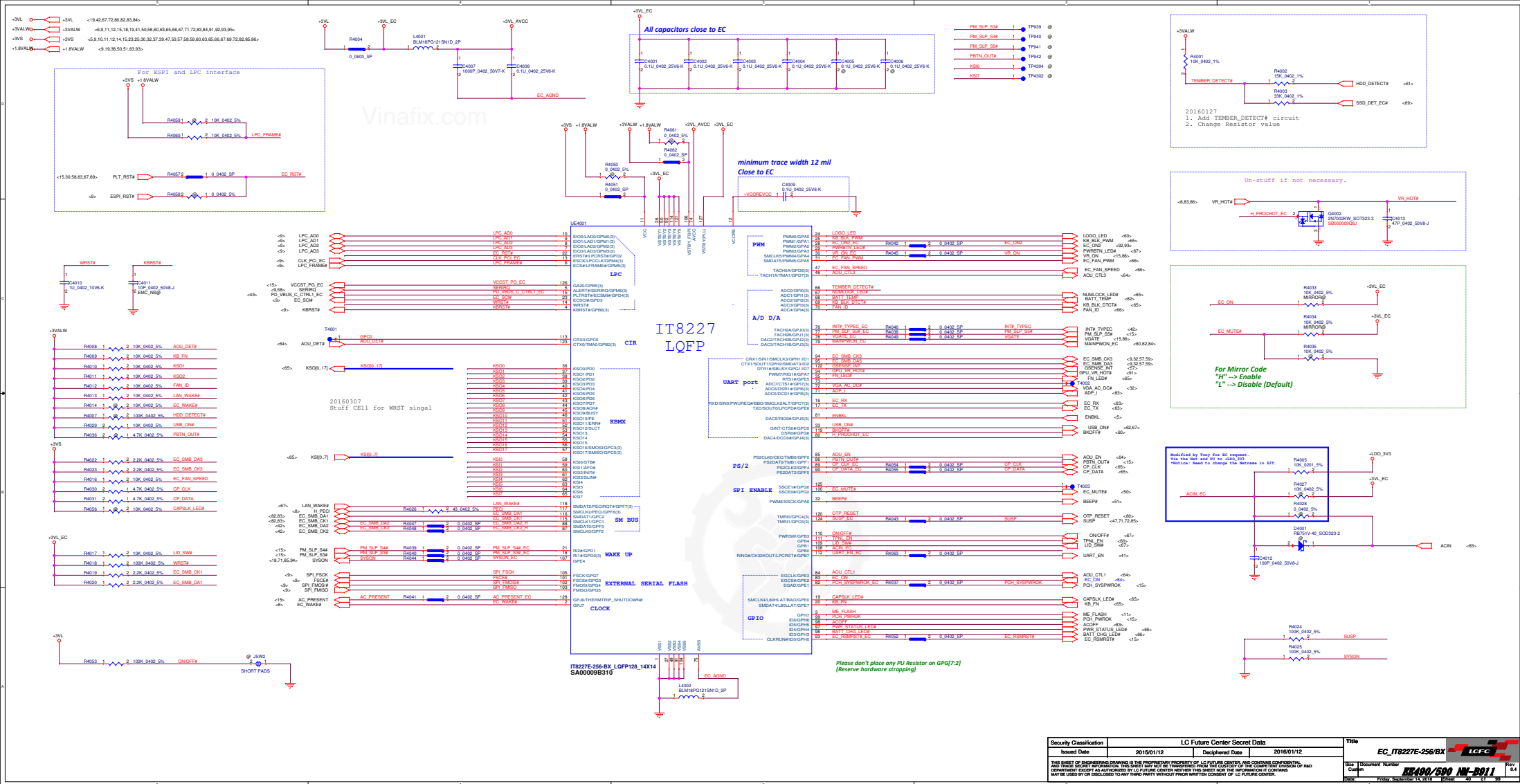



## +3VS to +3VS\_VGA



Discharge Circuit

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Units	EA500/590	NA-B911	
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Title		<b>AUDIO DEBUG PORT</b> 		Rev 0.
Size Custom	Document Number	<b>EE490/590 NM-B911</b>		
Date:	Friday, September 14, 2018	13:58	41	01

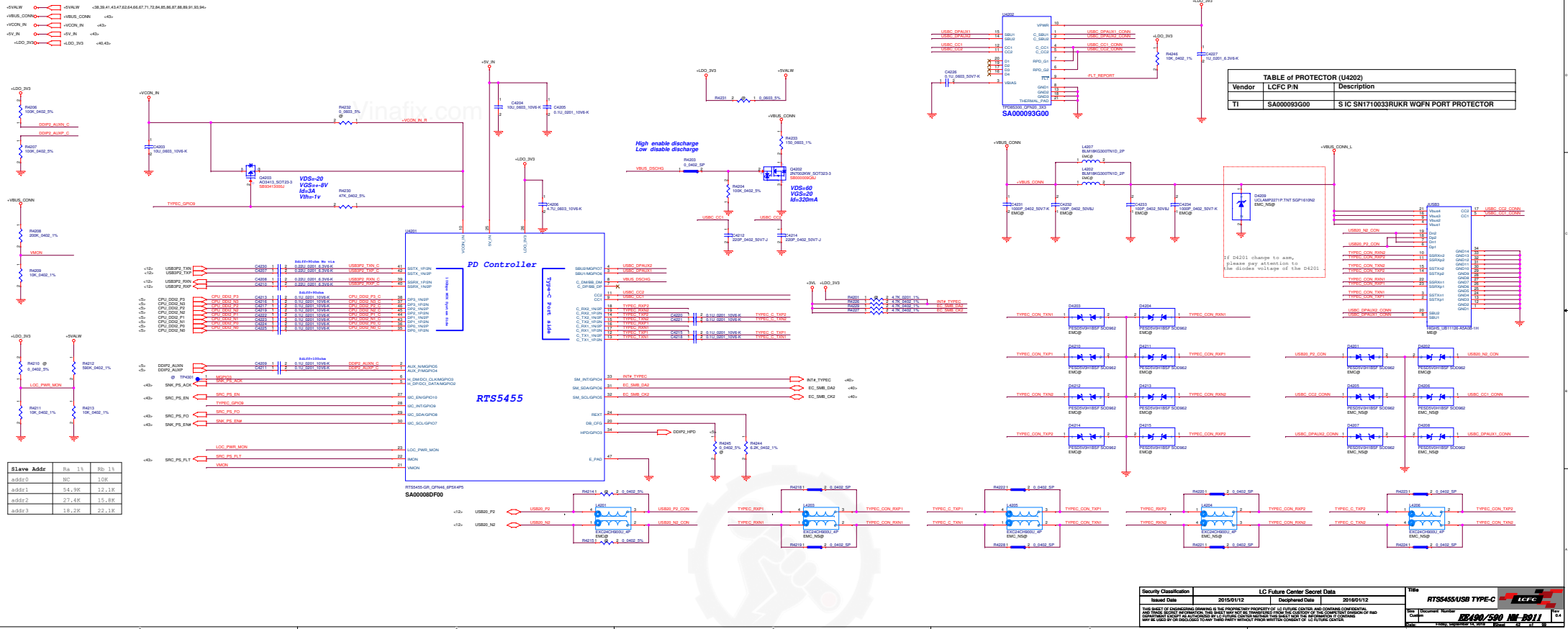


TABLE of PROTECTOR (U4202)		
Vendor	LCFC P/N	Description
TI	SA000093G00	S IC SN1710033RUKR WQFN PORT PROTECTOR



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+3VS +3VS <5.9,10,11,12,14,15,23,25,30,32,37,39,40,50,57,58,59,60,63,65,66,67,69,72,82,85,86>  
+5VS +5VS <41,50,51,60,61,65,66,72>  
B+ B+ <60,72,80,83,84,85,86,87,88,89,91,92,95>  
+5VALW +5VALW <38,39,41,42,43,62,64,66,67,71,72,84,85,86,87,88,89,91,93,94>

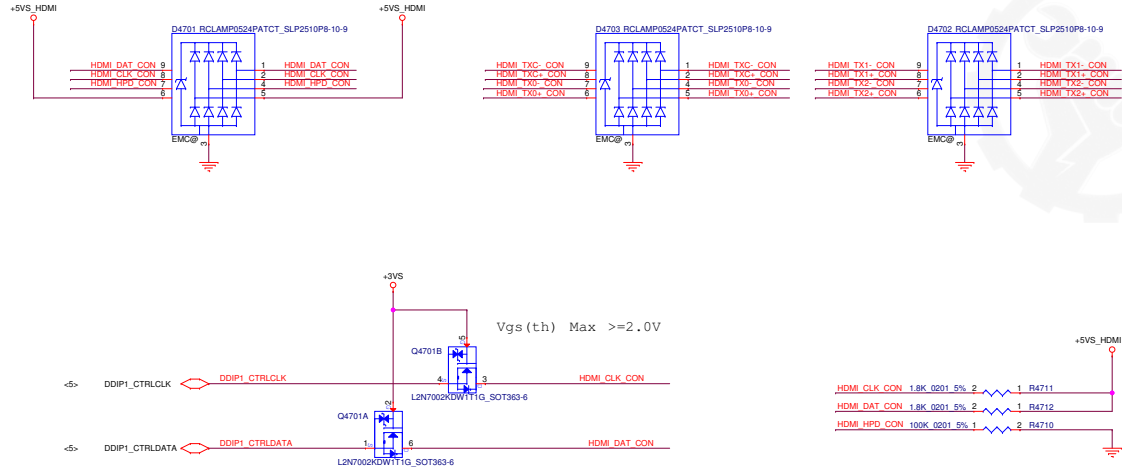
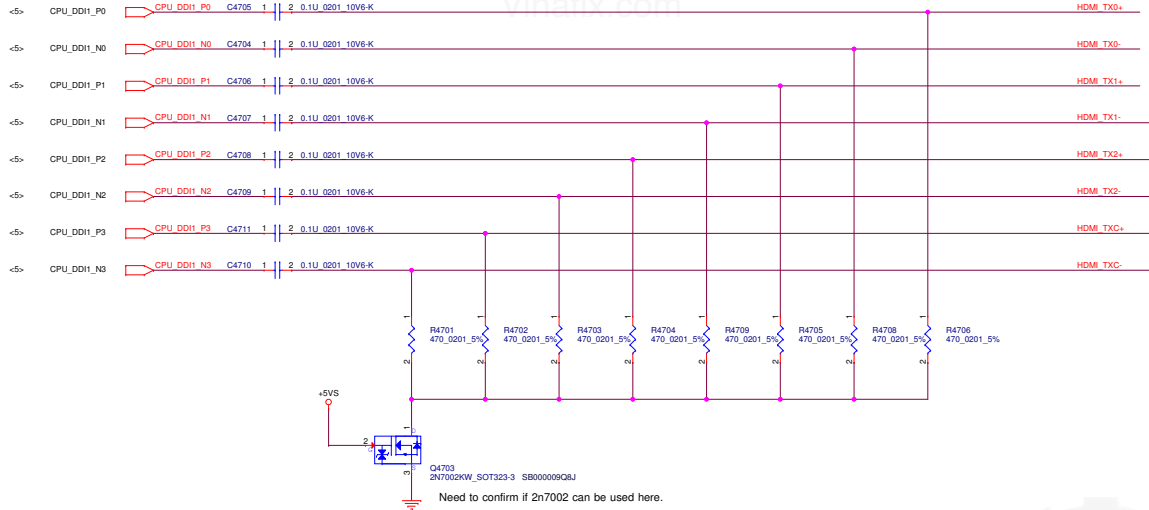


Figure 1-2. HDMI\* HPD Active Level Shifter Design Recommendation.

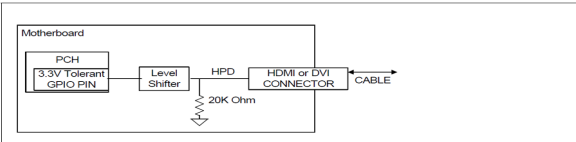


Figure 1-3. HDMI\* HPD Cost Reduced Level Shifter Design Recommendation.

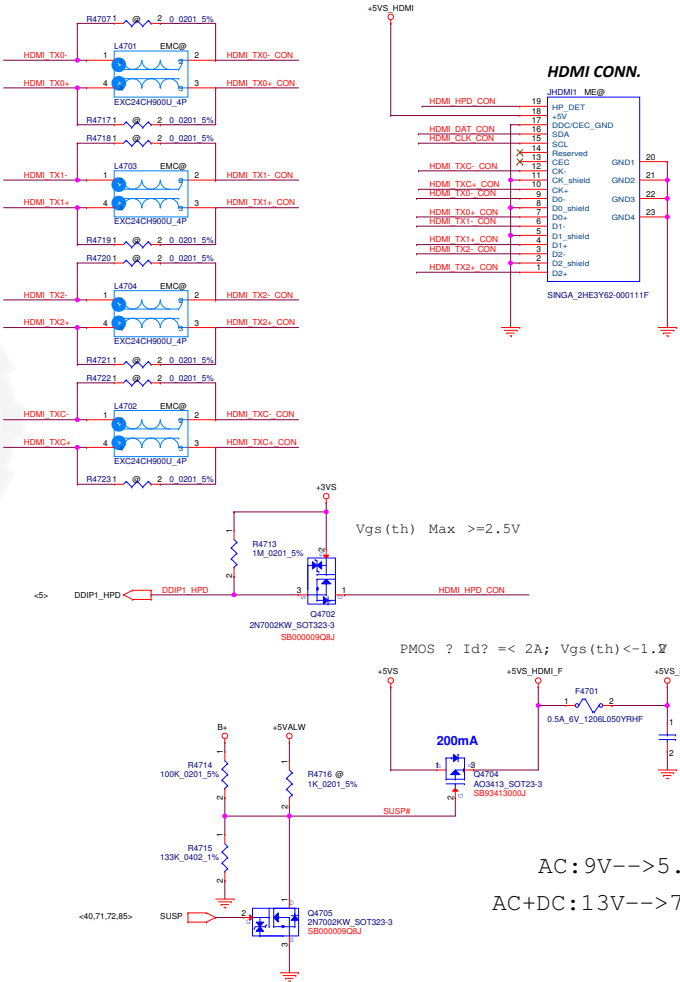
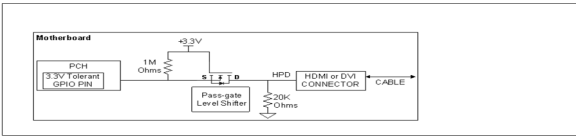


TABLE of POWER SWITCH (F4701)		
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LITTELFUSE SP040005G00	S FUSE 1206L050YRHF 0.5A 6V CURUS/TUV	
BOURNS SP040005L00	S_PPTC_TH MF-NSMF050-2 0.5A 13.2V UL/TUV	


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			Enclosure Number EE490/590 NW-B011
			Date Friday, September 11, 2016 07:08 49 01 39

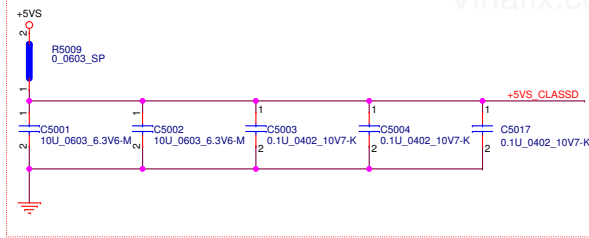
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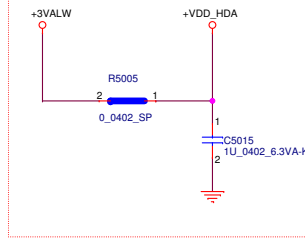
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Issued Date	2015/01/12	Deciphered Date	2016/01/12	BLANK		
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				Date:	Friday, September 14, 2018	Sheet 49 of 99

+5VS <41,47,51,60,61,65,66,72>  
+3VL <19,40,42,67,72,80,82,83,84>  
+3VALW <6,9,11,12,15,18,19,40,41,58,60,63,65,66,67,71,72,83,84,91,92,93,95>  
+1.8VALW <9,19,38,40,51,63,93>  
+MICBIAS <51>

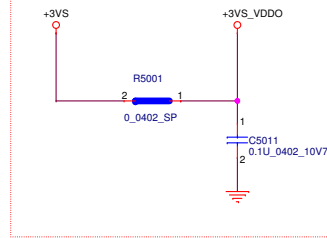
### Close to Pin13,16,29



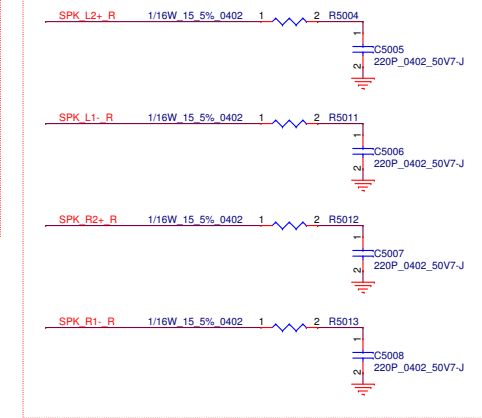
### Close to Pin3



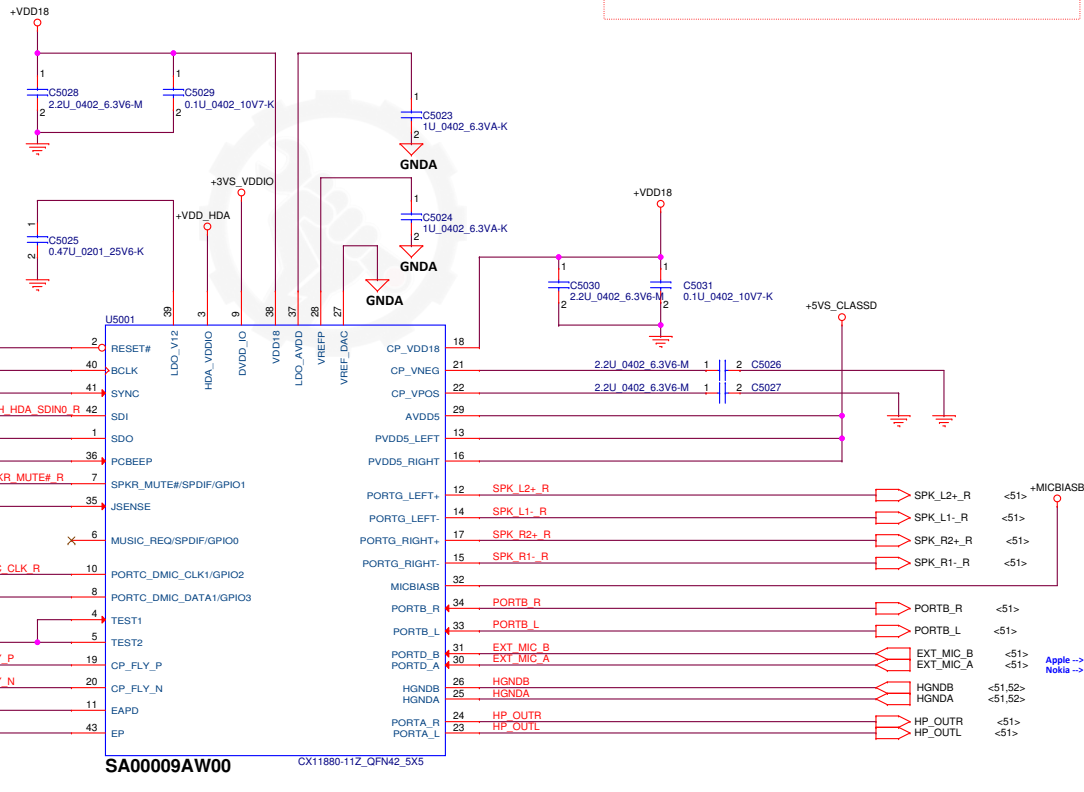
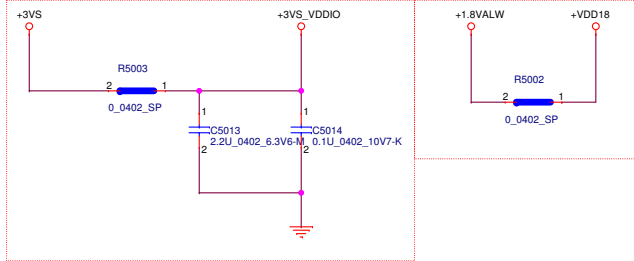
### Close to Pin7



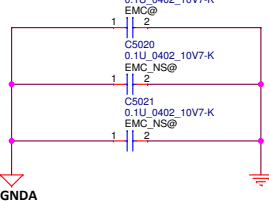
### EMI filter for Class D output signals Close to Codex



### Please Close to Pin9



W= 300mils

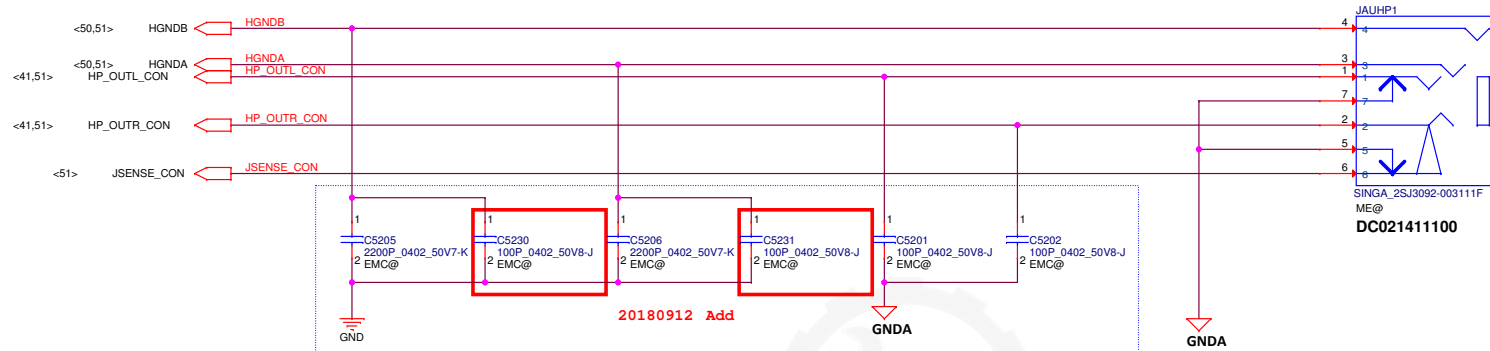


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Title		Size   Document Number		Date: Friday, September 14, 2016		Sheet 50 of 99	
CODEC-CX11880		EE490/590 NM-B911		Rev 0.4		Rev 0.4	

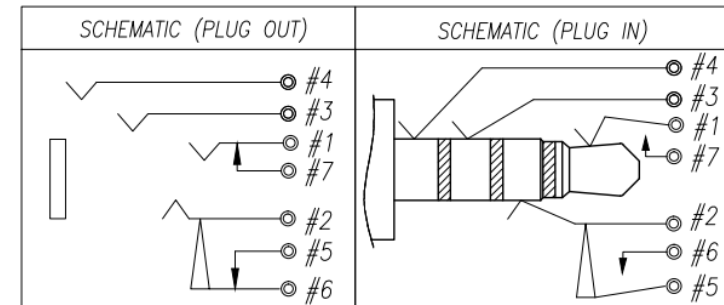
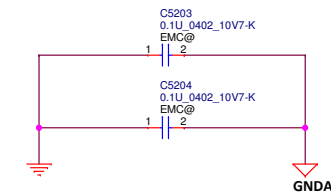
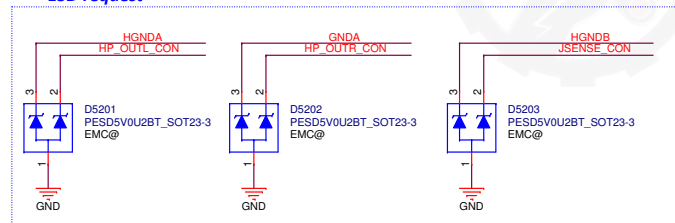






Vendor suggestion. Reserve for EMI.  
Close to JAUHP.


#### ESD request






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				Sheet	53 of 99
				Rev	0.4

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Issued Date	2015/01/12	Deciphered Date	2016/01/12	GBE LAN SWITCH(BLANK) 	
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				Sheet 35	01 99

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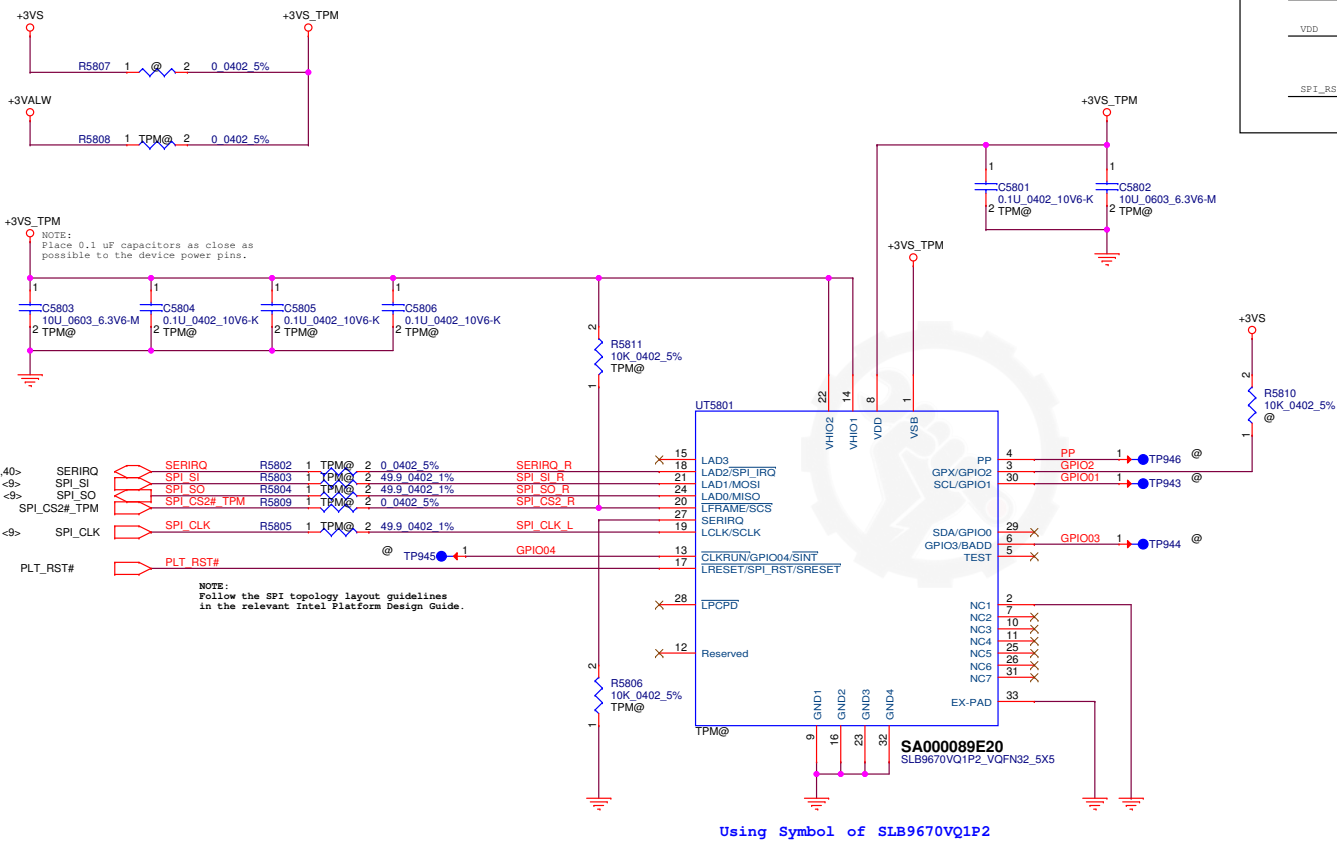
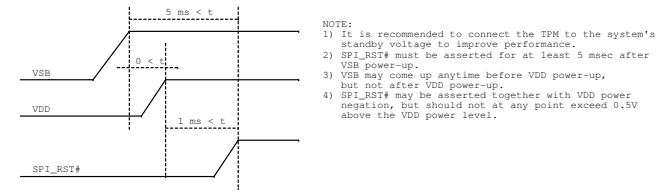


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				Date: Friday, September 14, 2018	Rev 0.4
				Sheet 36 of 99	



+3VS +3VS  
+3VALW +3VALW

NOTE:  
Check timing sequence in SDV phase.



Pin No	TCG PTP Spec (v38)	Infineon SLB9670VQ1.2 FW 6.10	ST Micro ST33HTPM2E32AAB9	Nuvoton NPC750LB0YX
1	VDD	VDD	NC	VSB
2	GND	GND	NC	NC
3	GPIO	NC	NC	GPX/GPIO2
4	GPIO	NC	PP	PP
5	NC	NC	NC	TEST
6	VNC/GPIO	GPIO	NC	GPIO3
7	GPIO/VDD	PP	GPIO	NC
8	VDD	VDD	NC	VDD
9	GND	GND	NC	GND
10	VNC	NC	NC	NC
11	NC	NC	NC	NC
12	NC	NC	NC	Reserved
13	VNC/GPIO	NC	NC	GPIO4
14	VDD	NC	NC	VDD
15	NC	NC	NC	DNC
16	GND	NC	NC	GND
17	SPI_RST#	RST#	SPI_RST#	SPI_RST#
18	SPI_PIRQ#	PIRQ#	SPI_PIRQ#	SPI_IRQ#
19	SPI_CLK	SCLK	SPI_CLK	SCLK
20	SPI_CS#	CS#	SPI_CS#	SCS#
21	MOSI	MOSI	MOSI	MOSI
22	VDD	VDD	VPS	VDD
23	GND	GND	NC	GND
24	MISO	MISO	MISO	MISO
25	NC	NC	NC	NC
26	NC	NC	NC	NC
27	NC	NC	NC	(SERIRQ)
28	NC	NC	NC	DNC
29	VNC/GPIO	NC	NC	GPIO0
30	VNC/GPIO	NC	NC	GPIO1
31	VNC	NC	NC	NC
32	GND	GND	NC	GND

Follow THP1\_SWG\_SIT\_EC005, update TPM table

TABLE of TPM (UT5801)		
Vendor	LCFC P/N	Description
ST	SA000089E20	S IC ST33HTPH2E32AHC0 VQFN 32P TPM
NUVOTON	SA00008KS10	S IC NPC750LABYX QFN 32P TPM

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### Thermal Sensor *Close to CPU*

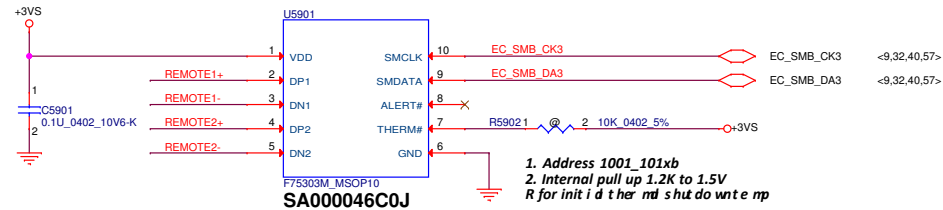
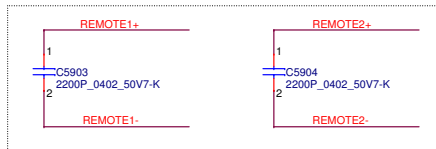
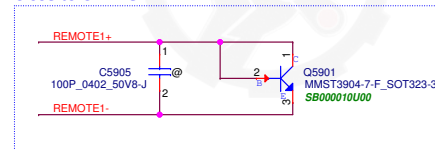


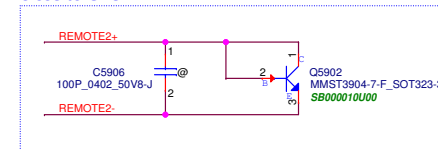
TABLE of Thermal Sensor (U5901)		
Vendor	P/N	LCFC P/N
FINTEK	F75303M	SA000046C0J
Nuvoton	NCT7719W	SA000065D00



### *Close to CHARGER*



### *Close to GPU*



Trace width/space:10/10 mil  
Trace length:<8"

+3VS <5,9,10,11,12,14,15,23,25,30,32,37,39,40,47,50,57,58,59,63,65,66,67,69,72,82,85,86>  
+5VS <41,47,50,51,61,65,66,72>  
+3VALW <6,9,11,12,15,18,19,40,41,50,58,63,65,66,67,71,72,83,84,91,92,93,95>

### LCDVDD Circuit

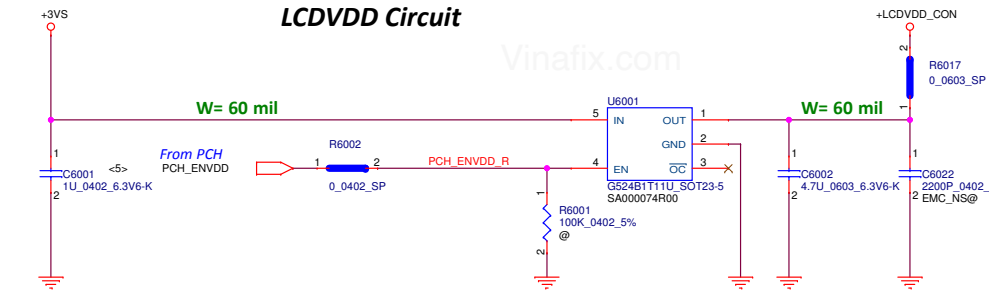
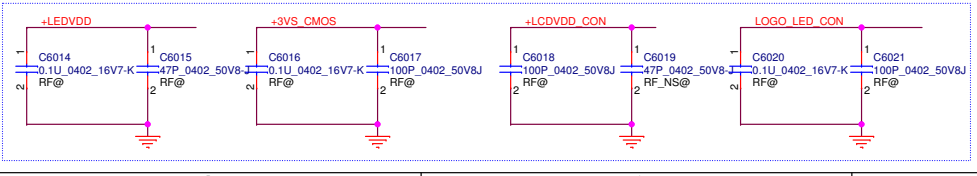
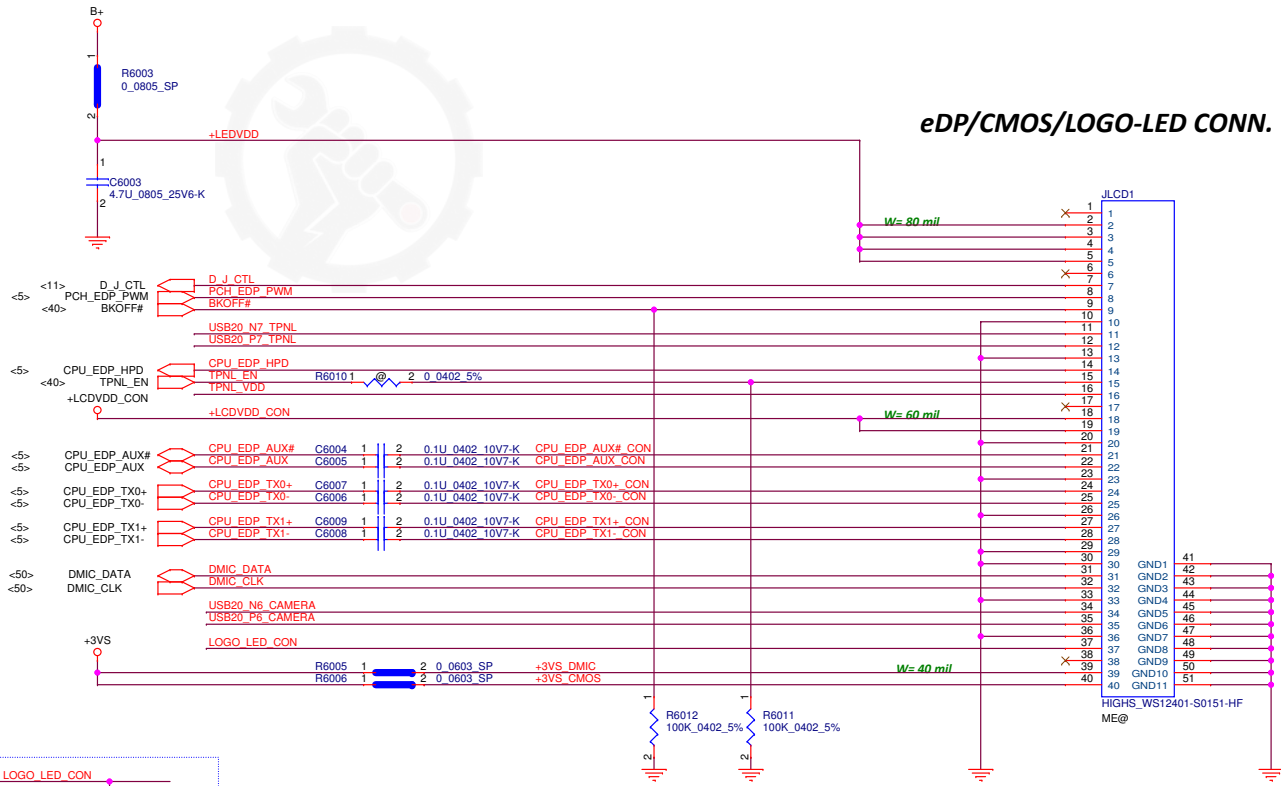
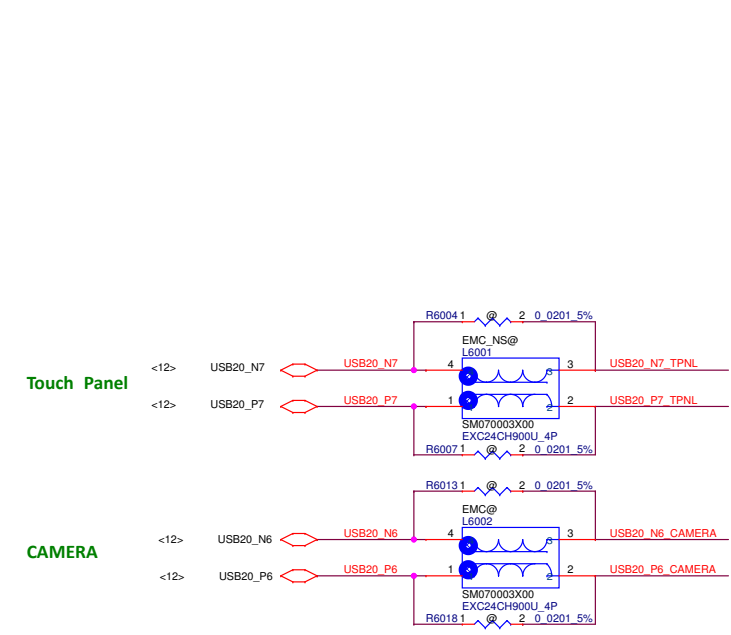
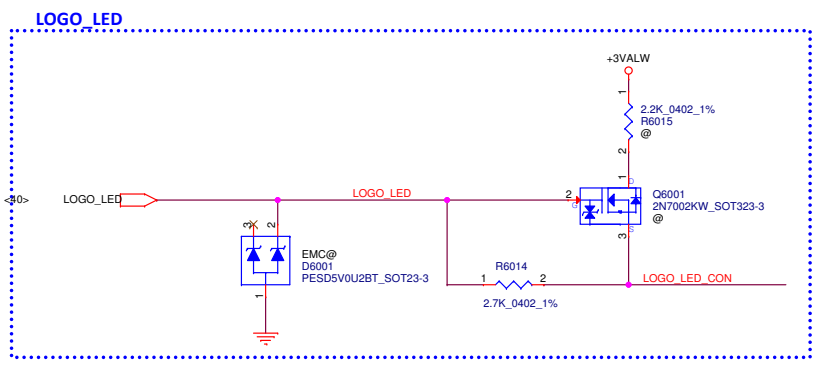
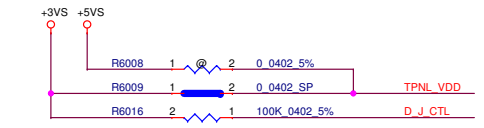


TABLE of POWER SWITCH (U6001)		
Vendor	LCFC P/N	Description
GMT	SA000074R00	S IC G524B1T11U SOT23 5P POWER SWITCH
SILERGY	SA000074P00	S IC SY6288C20AAC SOT23 5P POWER SWITCH

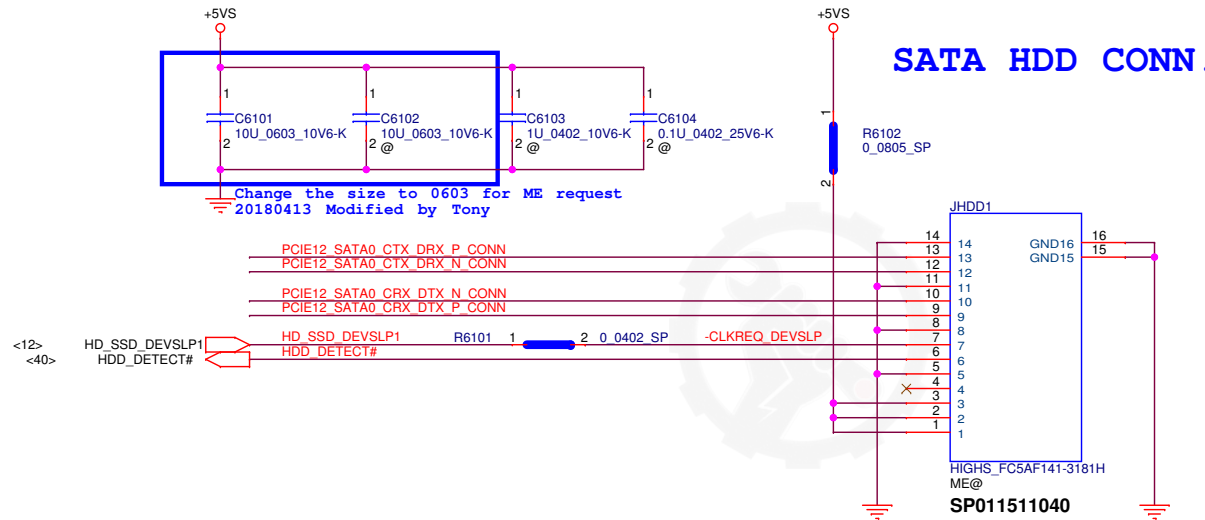




+5VS <41,47,50,51,60,65,66,72>

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<12>	PCIE12_SATA0_CTX_DRX_P	PCIE12_SATA0_CTX_DRX_P	C6112	1	2	0.01U_0201_6.3V7-K	PCIE12_SATA0_CTX_DRX_P_CONN
<12>	PCIE12_SATA0_CTX_DRX_N	PCIE12_SATA0_CTX_DRX_N	C6113	1	2	0.01U_0201_6.3V7-K	PCIE12_SATA0_CTX_DRX_N_CONN
<12>	PCIE12_SATA0_CRX_DTX_P	PCIE12_SATA0_CRX_DTX_P	C6114	1	2	0.01U_0201_6.3V7-K	PCIE12_SATA0_CRX_DTX_P_CONN
<12>	PCIE12_SATA0_CRX_DTX_N	PCIE12_SATA0_CRX_DTX_N	C6115	1	2	0.01U_0201_6.3V7-K	PCIE12_SATA0_CRX_DTX_N_CONN



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# On Board (LEFT-Front)

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+5VALW <38,39,41,42,43,47,64,66,67,71,72,84,85,86,87,88,89,91,93,94>  
+3VALW <6,9,11,12,15,18,19,40,41,50,58,60,63,65,66,67,71,72,83,84,91,92,93,95>  
+USB\_PWR\_S2

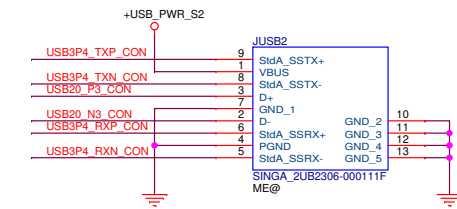
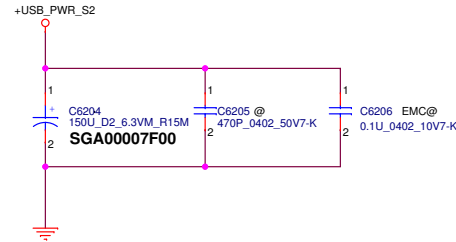
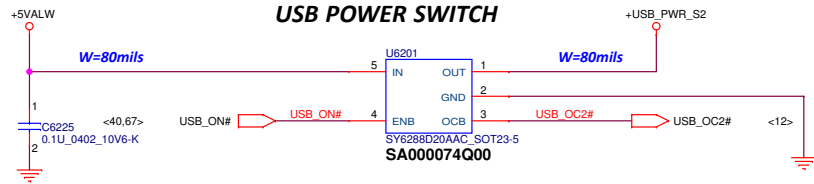
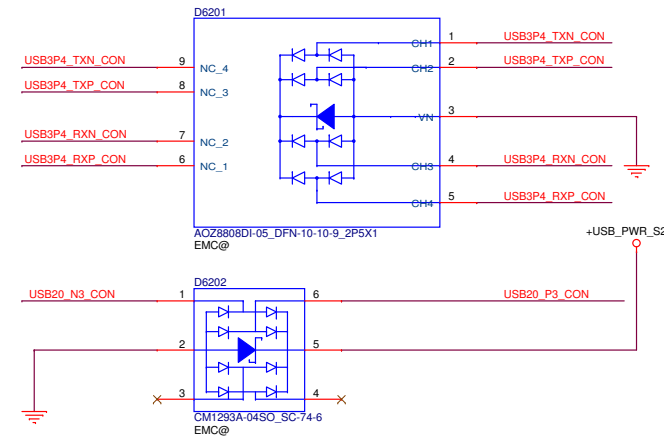
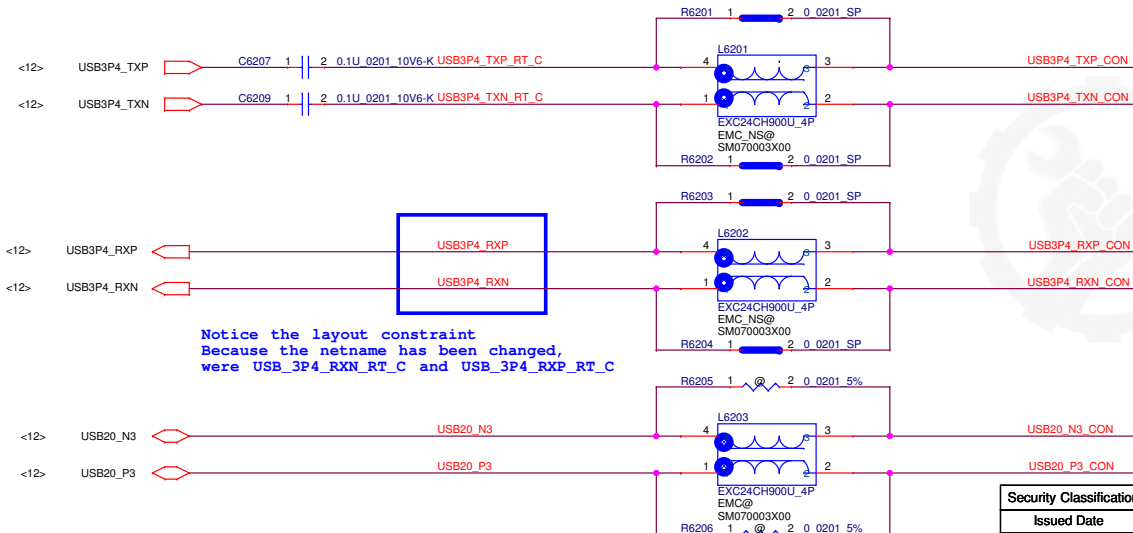


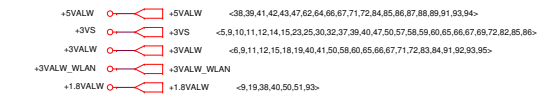
TABLE of POWER SWITCH (U6201)

Vendor	LCFC P/N	Description
SILERGY	SA000074Q00	S IC SY6288D20AAC SOT23 5P POWER SWITCH
GMT	SA000079400	S IC G517F2T11U SOT-23 5P POWER SWITCH



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Title		LCFC	
USB3 P2 CONN		EE490/590 NM-B911	
Size	Document Number	Rev	
Custom		0.4	
Date:	Friday, September 14, 2018	Sheet	62 of 99



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# KEY-E NGFF CCARD FOR WLAN

H=3.20mm Connector

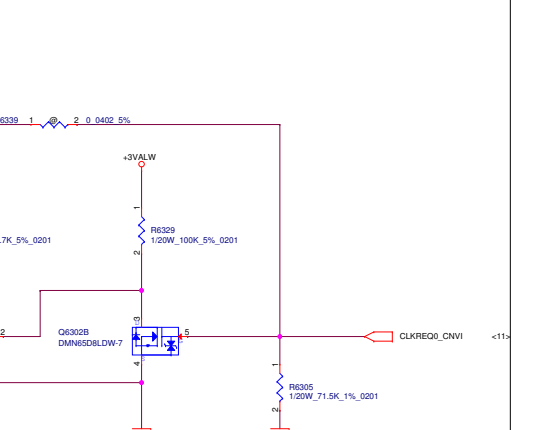
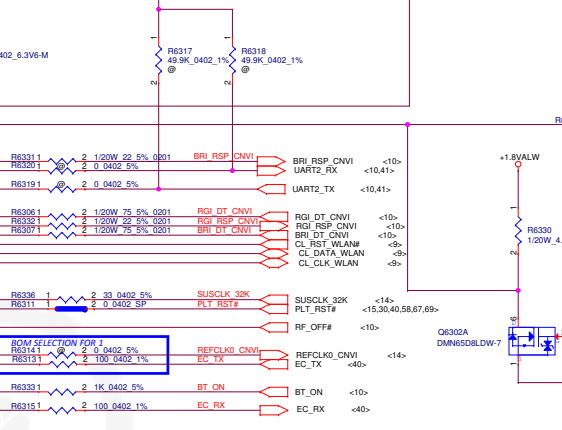
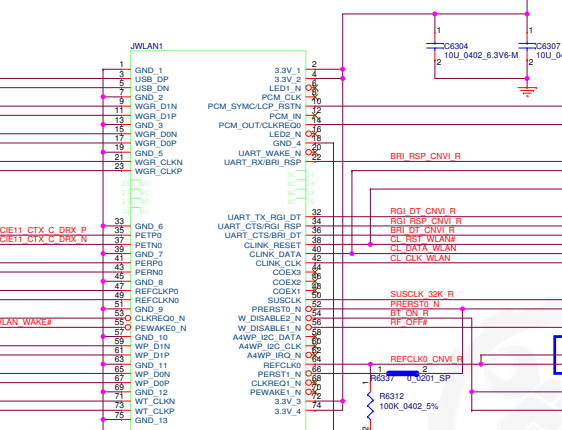
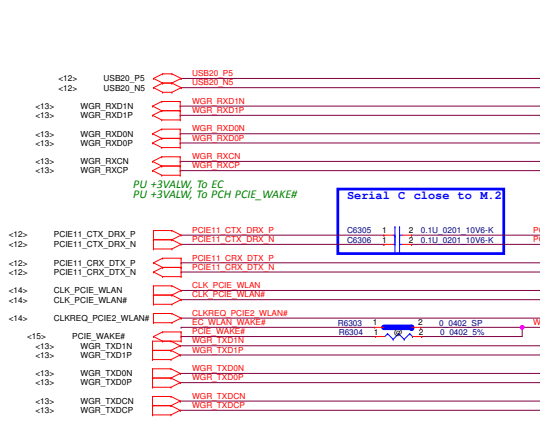
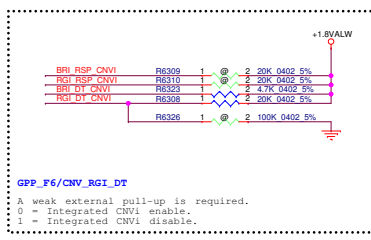
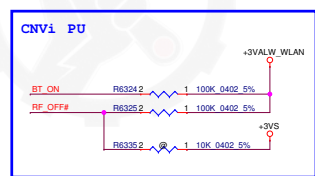


Figure 9-3. Hybrid Key-E Pinout- Platform Side View

Standard M.2 Key E	LCFC Signals	LCFC Signals	Standard M.2 Key E
74	+V3P3A	WT_CLKP	REFCLKN1
72	+V3P3A	WT_CLKN	REFCLKP1
70	PEWake1(I/O)(0/3.3V)		
68	CLKREQ1(I/O)(0/3.3V)	WT_DOP	PERn1
66	FURST1(I/O)(0/3.3V)	WT_DON	PERp1
64	RESERVED	REFCLK0(I/O)(0/3.3V)	
62	ALERTN(I/O)(1.8V)	A4WP_IRQ#	
60	I2C_CLK(I/O)(0/1.8V)	A4WP_I2C_CLK	WT_DIP
58	I2C_DATA(I/O)(0/1.8V)	A4WP_I2C_DATA	WT_DIN
56	W_DISABLE1(I/O)(0/3.3V)		
54	W_DISABLE2(I/O)(0/3.3V)		
52	PERST0(I/O)(0/3.3V)	PEWake0(I/O)(0/3.3V)	
50	SUSCLK(32MHz)(I/O)(0/3.3V)	CLKREQ0(I/O)(0/3.3V)	
48	COEX_TXD(I/O)(0/1.8V)		
46	COEX_RXD(I/O)(0/1.8V)		
44	COEX3(I/O)(0/1.8V)		
42	CLKM_CLK		
40	CLKM_DATA		
38	CLKM_RESET(I/O)(0/3.3V)		
36	LPSS_UART1_TX(I/O)(0/1.8V)	BRI_RSP_CNVI	
34	LPSS_UART1_TX(I/O)(0/1.8V)	RGI_DT_CNVI	
32	LPSS_UART1_TX(I/O)(0/1.8V)	RST_DT_CNVI	
Connector Key			
Connector Key			
Connector Key			
Connector Key			
22	LPSS_UART1_TX(I/O)(0/1.8V)	WGR_CLKP	SDIO_Reset(I/O)(0/1.8V)
20	UART_WAKE#(I/O)(1.8V)	WGR_CLKN	SDIO_Wake(I/O)(0/1.8V)
18	GND	GND	SDIO_DATA1(I/O)(0/1.8V)
16	GND	GND	SDIO_DATA2(I/O)(0/1.8V)
14	PCM_OUT(I/O)(0/1.8V)	WGR_DOP	SDIO_DATA3(I/O)(0/1.8V)
12	PCM_IN(I/O)(0/1.8V)	WGR_DON	SDIO_DATA4(I/O)(0/1.8V)
10	PCM_SYNC(I/O)(0/1.8V)	WGR_DIP	SDIO_CMD0(I/O)(0/1.8V)
8	PCM_CLK(I/O)(0/1.8V)	WGR_DIN	SDIO_CLK0(I/O)(0/1.8V)
6	LED1(I/O)(0/1.8V)		
4	+V3P3A		
2	+V3P3A		

TABLE OF WLAN(JWLAN1)		
Vendor	P/N	LCFC P/N
TE	TE_1-2199119-1_75P-T	SP021703091



# On Board (LEFT-Back)

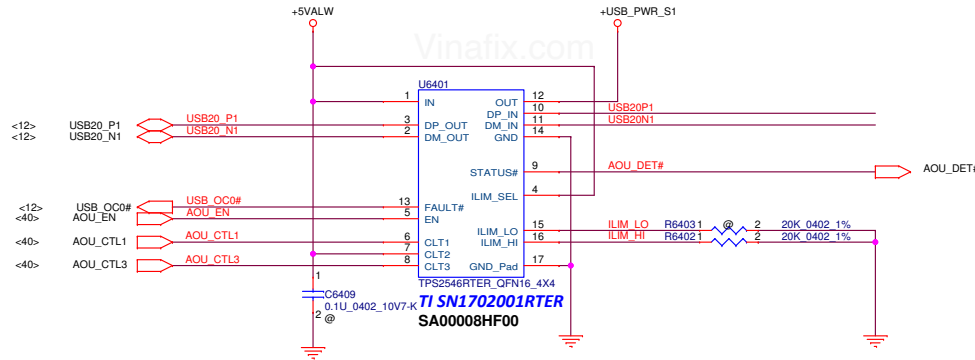
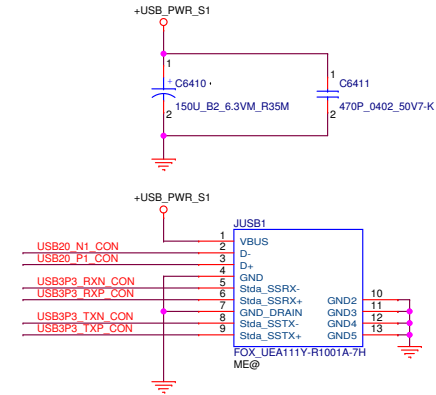
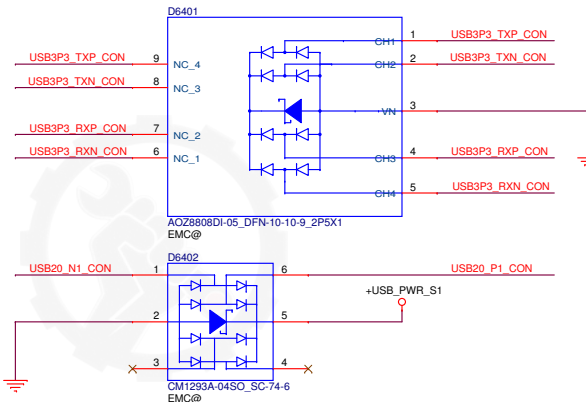



TABLE of POWER SWITCH (U6401)

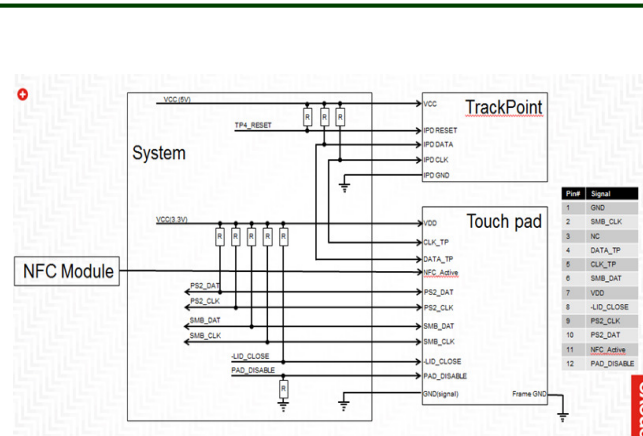
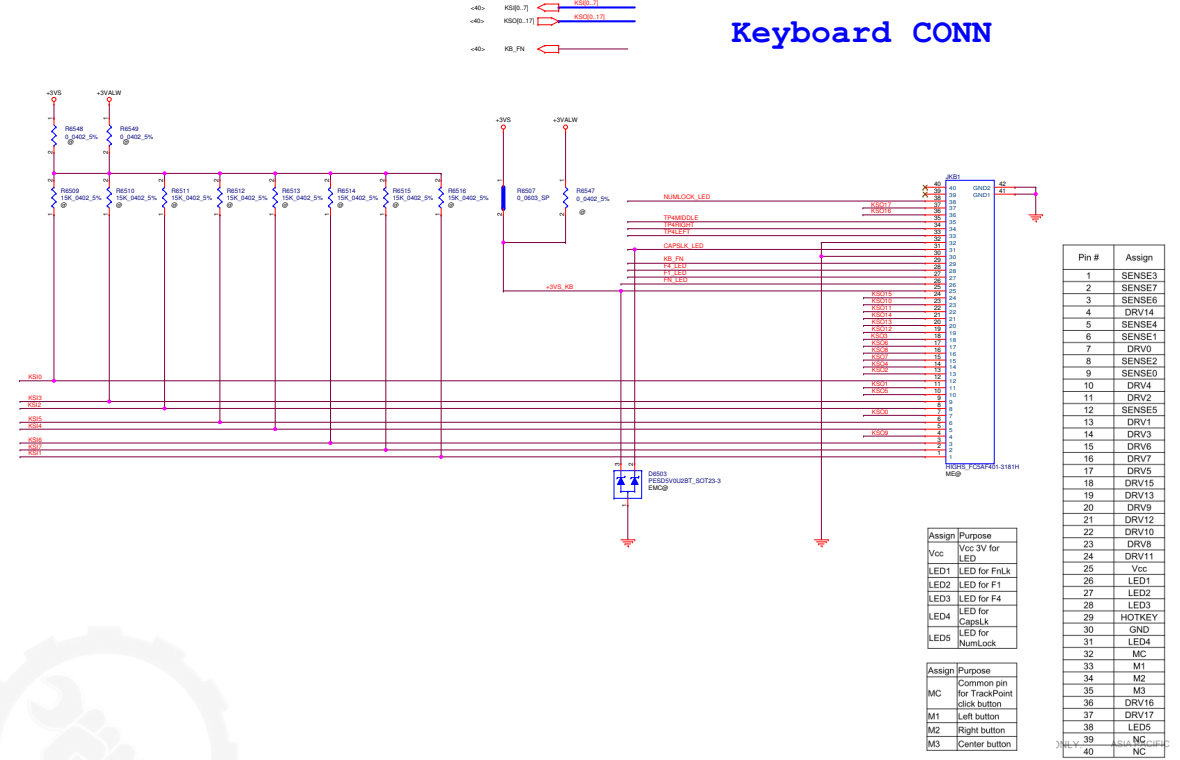
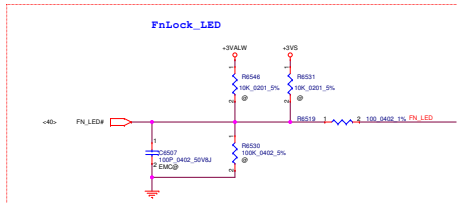
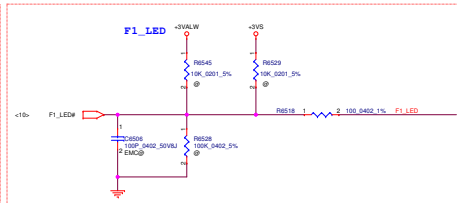
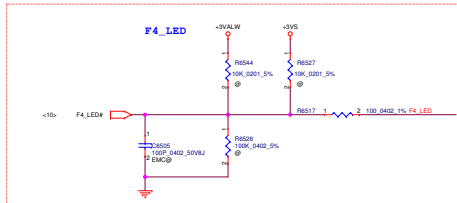
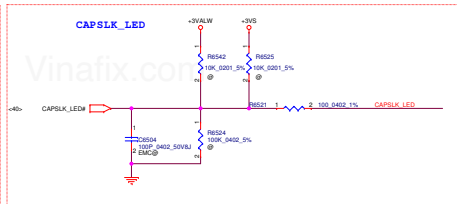
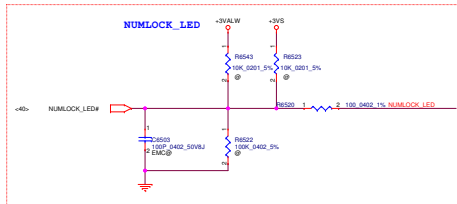
Vendor	LCFC P/N	Description
TI	SA00008HF00	S IC SN1702001RTER WQFN 16P USB CHARGING
DIODES	SA00009D800	S IC PI5USB2546HZHEX TQFN 16P CONTROLLER

CLT1	CLT2	CLT3	ILIM_SEL	MOD
0	0	0	X	DCH OUT held low
1	1	1	1	CDP Data Connected and Port Power Mgt. Function Active
1	1	1	0	SDP2 Data Connected
1	1	0	X	SDP1 Data Connected
0	1	0	X	SDP1 Data Connected
1	0	0	X	DCP_Short Device Forced to stay in DCP BC 1.2 charging mode
1	0	1	X	DCP_Divider Device Forced to stay in DCP Divider 1 Charging Mode
0	1	1	X	DCP_Auto Data Disconnected and Port Power Mgt. Function Active
0	0	1	X	DCP_Auto Data Disconnected and Power Wake Function Active

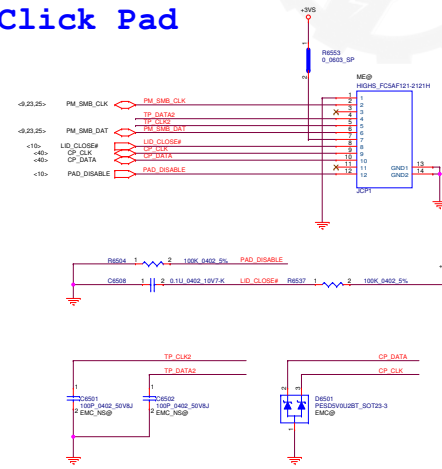


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+3VS +3VS -41.47,56.51,66.81,66.72-  
 +3VS +3VS -5.9,16.11,12.14,15.23,25.30,32.37,39,40,47,50.57,58.59,60.63,66.67,69.72,82,85,96-  
 +3VALW +3VALW -6.9,11,12.15,16,18,40,41,50,59,60.63,66.67,71,72,83,84,91,92,93,95-

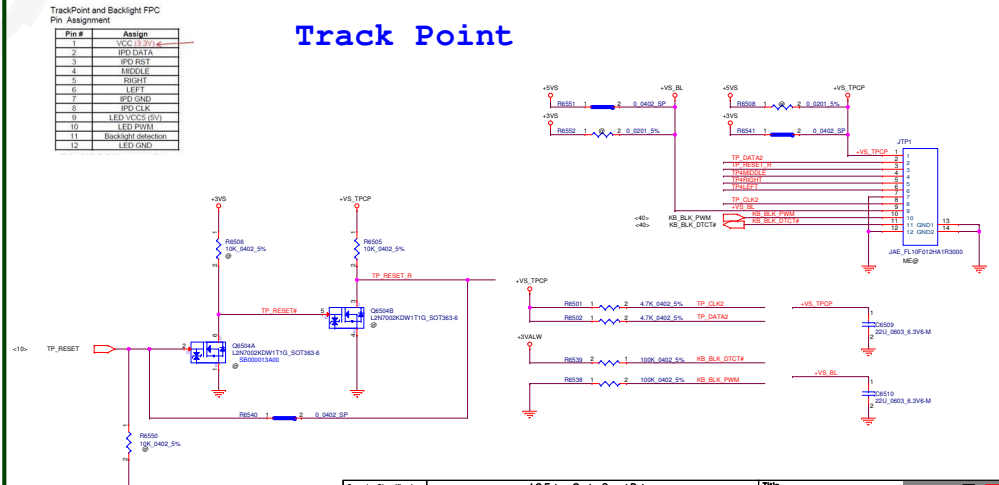


## Click Pad



Pin #	Assign
1	TP_RESET
2	TP_CLK
3	TP_DATA
4	TP_DATA
5	TP_DATA
6	TP_DATA
7	TP_DATA
8	TP_DATA
9	TP_DATA
10	TP_DATA
11	TP_DATA
12	TP_DATA

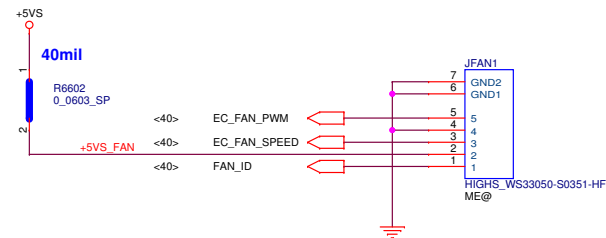
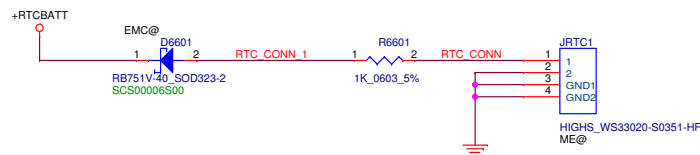
## Track Point



+RTCBATT <14,80>  
+5VS <41,47,50,51,60,61,65,72>  
+3VS <5,9,10,11,12,14,15,23,25,30,32,37,39,40,47,50,57,58,59,60,63,65,67,69,72,82,85,86>  
+3VALW <6,9,11,12,15,18,19,40,41,50,58,60,63,65,67,71,72,83,84,91,92,93,95>

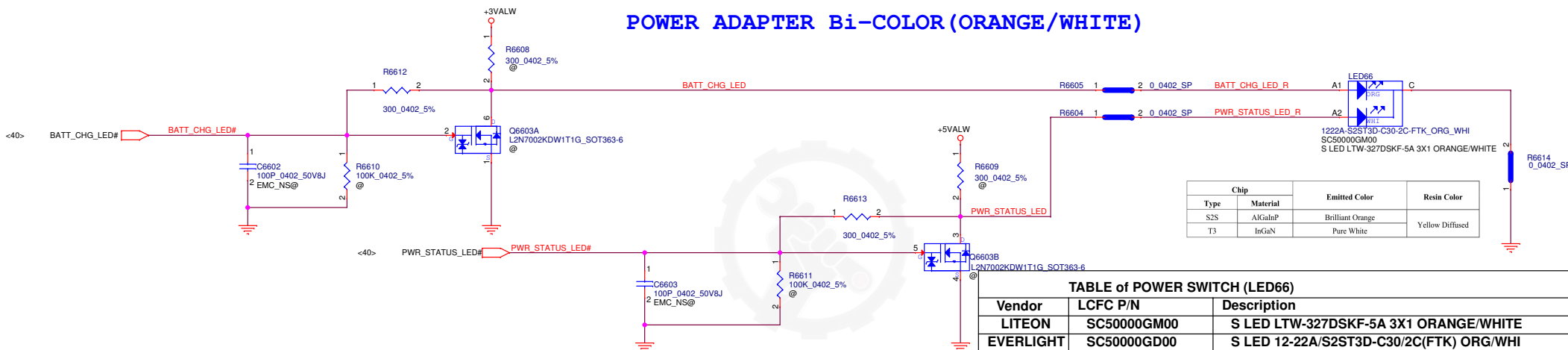
## RTC CONN.

## FAN CONN.



Pin No.	Signal	Note
1	ID	Fan ID
2	VCC	+5V
3	FG	2 Pulses
4	GND	-
5	PWM	PWM

## POWER ADAPTER Bi-COLOR (ORANGE/WHITE)

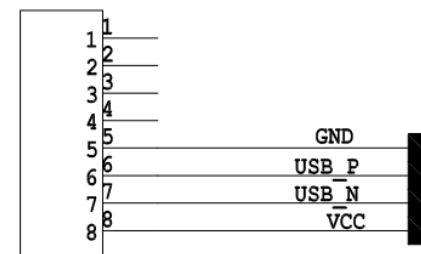
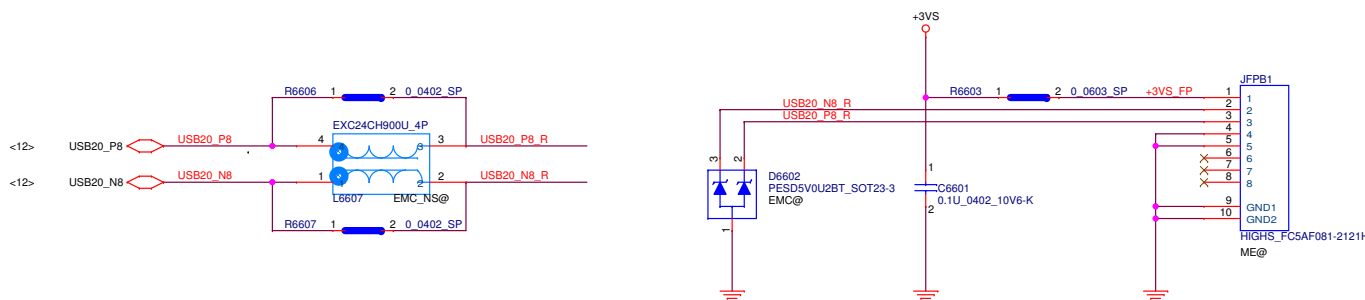


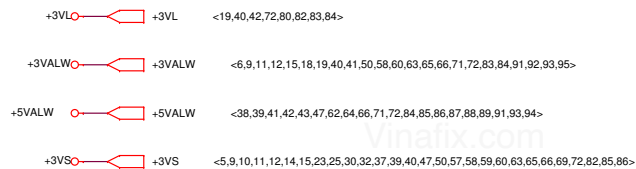
Chip	Type	Material	Emitted Color	Resin Color
S2S	T3	AlGaInP	Brilliant Orange	Yellow Diffused
		InGaN	Pure White	

TABLE of POWER SWITCH (LED66)

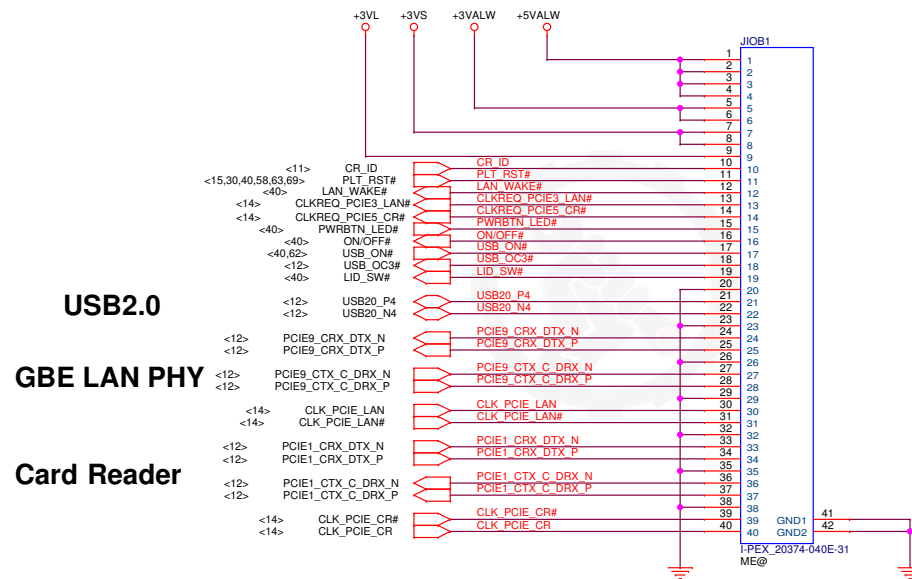
Vendor	LCFC P/N	Description
LITEON	SC50000GM00	S LED LTW-327DSKF-5A 3X1 ORANGE/WHITE
EVERLIGHT	SC50000GD00	S LED 12-22A/S2ST3D-C30/2C(FTK) ORG/WHI

## FingerPrint CONN.






## IO\_40\_Pin conn



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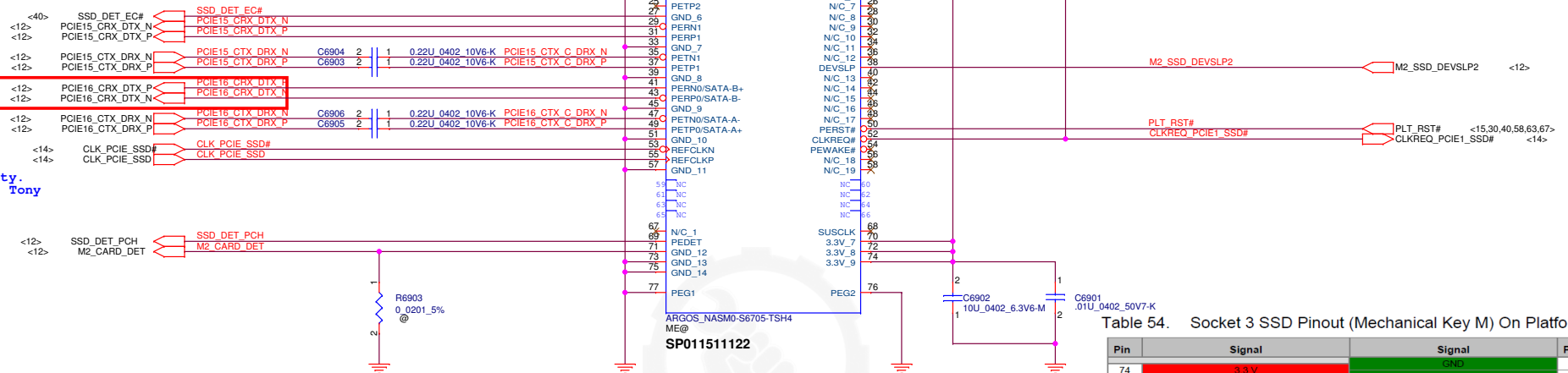
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# M.2 SSD(M TYPE)

## 6.5.4.1.1 AC Capacitor General Guidelines SATA / PCI Express\* Multiplexed Ports

The following table summarizes the AC capacitor requirements on the motherboard when using the SATA/PCIe\* multiplexed ports. **When SATA and PCIe are muxed, always route according to SATA design guidelines.** SATA does not support signal polarity reversal and does not support lane reversal.



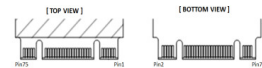
Swap for SATA polarity.  
20180514 Modified by Tony

Table 6-16. SATA / PCI Express\* Gen 2 and Gen 3 Capacitor Values (Sheet 1 of 2)

Condition	PCI Express* Gen 2 Only	PCI Express* Gen 3 Only	SATA Only	PCI Express* Gen 2/ SATA	PCI Express* Gen 3/ SATA
Processor Tx	100 nF	220 nF	10 nF	100 nF	220 nF
Processor Rx	None	None	10 nF <sup>1</sup>	None <sup>2</sup>	None <sup>3</sup>

### 4.0 Electrical Interface Specification (TBD)

#### 4.1 Serial ATA Interface Connector



#### 4.2 Pin Assignments

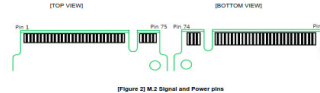
Pin#	Assignment	Description	Pin#
76	3.3V	GND	75
72	3.3V	GND	71
70	3.3V	GND	69
68	NC	NC	67
66	Module Key	Module Key	65
64	Module Key	Module Key	63
62	Module Key	Module Key	61
60	NC	NC	59
58	NC	NC	57
56	NC	NC	55
54	NC	NC	53
52	NC	NC	51
50	NC	SATA-A+	49
48	NC	SATA-A-	47
46	NC	SATA-B	45
44	NC	SATA-B	43
42	NC	SATA-B+	41
40	NC	GND	39
38	DEVSLP	NC	37
36	NC	NC	35
34	NC	NC	33
32	NC	NC	31
30	NC	NC	29
28	NC	NC	27
26	NC	NC	25
24	NC	NC	23
22	NC	NC	21
20	NC	Module Key	19
18	Module Key	Module Key	17
16	Module Key	Module Key	15
14	Module Key	Module Key	13

IF THERE IS ANY OTHER OPERATION TO IMPLEMENT IN ADDITION TO SPECIFICATION IN THE DATASHEET OR JEDEC STANDARD, PLEASE CONTACT EACH BRANCH OFFICE OR HEADQUARTERS OF SAMSUNG ELECTRONICS.

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### 4.0 INTERFACE SPECIFICATION

#### 4.1 Connector Dimension and Pin Location



#### 4.2 Pin Assignments and Definition

Pin#	Assignment	Description	Pin#	Assignment	Description
1	GND	Return current path	2	3.3V	3.3V source
3	GND	Return current path	4	3.3V	3.3V source
5	PETx3	PCIe Tx	6	NC	NC
7	PETx3	PCIe Tx	8	NC	NC
9	GND	Return current path	10	LD18	Device Active Signal (Refer to Table 11)
11	PERx3	PCIe Rx	12	3.3V	3.3V source
13	PERx3	PCIe Rx	14	3.3V	3.3V source
15	GND	Return current path	16	3.3V	3.3V source
17	PETx3	PCIe Tx	18	3.3V	3.3V source
19	PETx3	PCIe Tx	20	NC	NC
21	GND	Return current path	22	NC	NC
23	PERx3	PCIe Rx	24	NC	NC
25	PERx3	PCIe Rx	26	NC	NC
27	GND	Return current path	28	NC	NC
29	PETx3	PCIe Tx	30	NC	NC
31	PETx3	PCIe Tx	32	NC	NC
33	GND	Return current path	34	NC	NC
35	PERx3	PCIe Rx	36	NC	NC
37	PERx3	PCIe Rx	38	NC	NC
39	GND	Return current path	40	ALTRN0(1)	DRN0 (Do Not Use)
41	PETx3	PCIe Tx	42	SMB_DATA(SDP)	DRN0 (Do Not Use)
43	PETx3	PCIe Tx	44	SMB_CLK(SDP)	DRN0 (Do Not Use)
45	GND	Return current path	46	NC	NC
47	PERx3	PCIe Rx	48	NC	NC
49	PERx3	PCIe Rx	50	PERST#	PCIe Reset
51	GND	Return current path	52	CLKREQ#	PCIe Device Clock Request
53	REFCLKN	PCIe Reference Clock	54	PEWAKE#	NC
55	REFCLKP	PCIe Reference Clock	56	REFCLKP	NC
57	GND	Return current path	58	REFCLKP	NC
59	NC	NC	60	SUSCLK	DRN0 (Do Not Use)
61	NC	NC	62	NC	NC
63	NC	NC	64	NC	NC
65	NC	NC	66	NC	NC
67	NC	NC	68	NC	NC
69	NC	NC	70	NC	NC
71	NC	NC	72	3.3V	3.3V source

IF THERE IS ANY OTHER OPERATION TO IMPLEMENT IN ADDITION TO SPECIFICATION IN THE DATASHEET OR JEDEC STANDARD, PLEASE CONTACT EACH BRANCH OFFICE OR HEADQUARTERS OF SAMSUNG ELECTRONICS.

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Table 54. Socket 3 SSD Pinout (Mechanical Key M) On Platform


Pin	Signal	Signal	Pin
74	3.3 V	GND	75
72	3.3 V	GND	73
70	3.3 V	GND	71
68	PEDET (NC-PCIe/GND-SATA)	NC	69
66	SUSCLK(32kHz) (I/O)(0/3.3V)	CONNECTOR Key M	67
64	CONNECTOR Key M	CONNECTOR Key M	63
62	CONNECTOR Key M	CONNECTOR Key M	61
60	CONNECTOR Key M	CONNECTOR Key M	59
58	NC	GND	57
56	NC	REFCLKp	55
54	PEWAKE# (I/O)(0/3.3V) or NC	REFCLKn	53
52	CLKREQ# (I/O)(0/3.3V) or NC	GND	51
50	PERST# (I/O)(0/3.3V) or NC	PETp0/SATA-A+	49
48	NC	PETn0/SATA-A-	47
46	NC	PERp0/SATA-B-	45
44	ALERT# (I) (0/1.8V)	PERn0/SATA-B+	43
42	SMB_DATA (I/O) (0/1.8V)	GND	41
40	SMB_CLK (I/O) (0/1.8V)	GND	39
38	DEVSLP (O)	PETp1	37
36	NC	PETn1	35
34	NC	GND	33
32	NC	PERp1	31
30	NC	PERn1	29
28	NC	GND	27
26	NC	PETp2	25
24	NC	PETn2	23
22	NC	GND	21
20	NC	PERp2	19
18	3.3 V	PERn2	17
16	3.3 V	GND	15
14	3.3 V	PETp3	13
12	3.3 V	PETn3	11
10	DAS/DSS (I/O)/LED_1# (I)(0/3.3V)	PERp3	9
8	NC	PERn3	7
6	NC	GND	5
4	3.3 V	GND	3
2	3.3 V	GND	1

\*Notice the Pin#43 and 41 for SATA and PCIe Combo Port.  
Refer to PCI Express M.2 Specification

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		Rev	0.4

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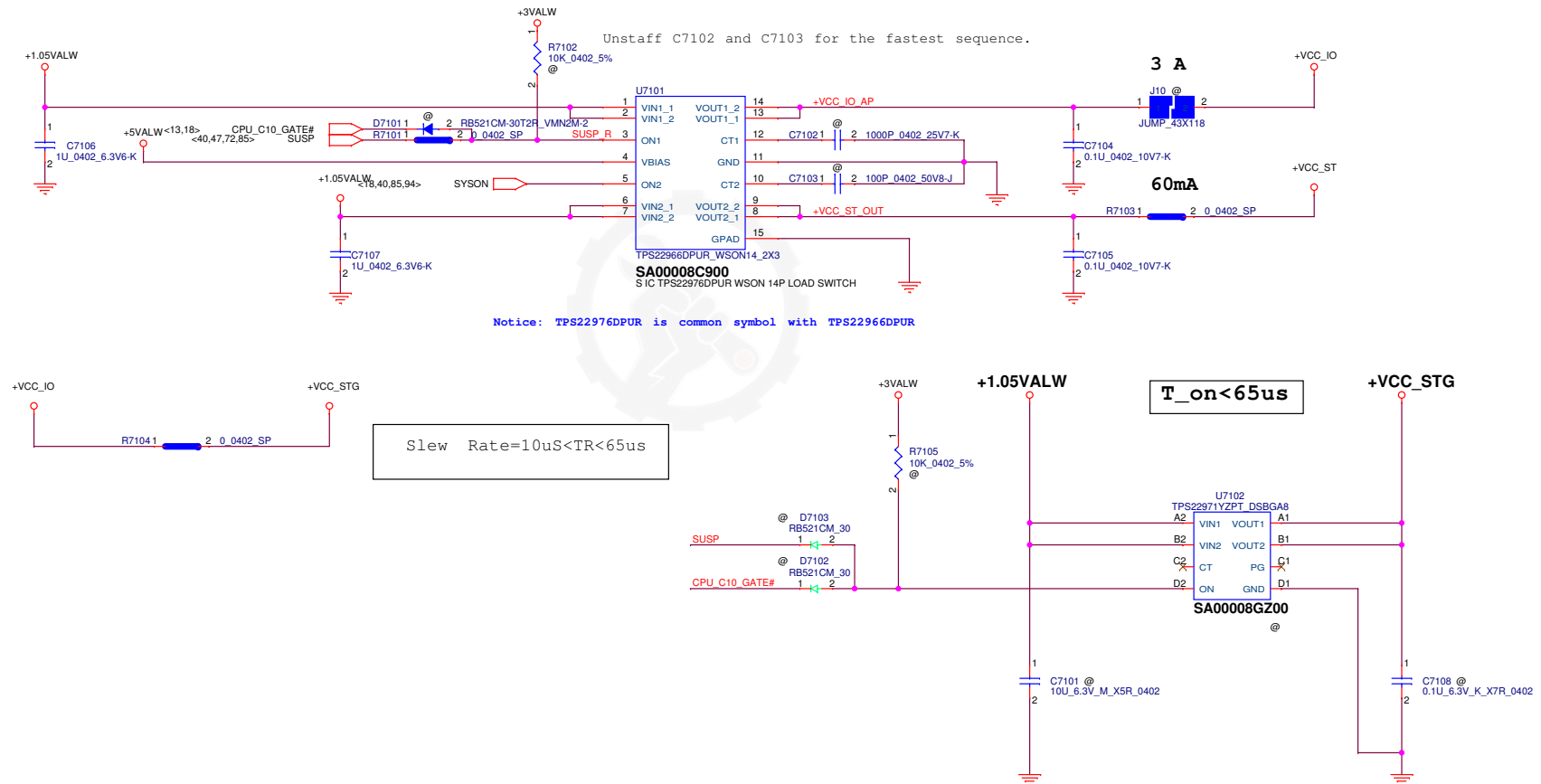


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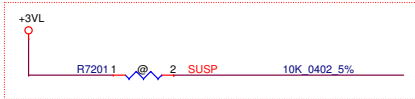
+1.05VALW		+1.05VALW	<19,21,92>
+VCC_STG		+VCC_STG	<8,16,18>
+VCC_IO		+VCC_IO	<5,11,18,21>
+5VALW		+5VALW	<38,39,41,42,43,47,62,64,66,67,72,84,85,86,87,88,89,91,93,94>
+VCC_ST		+VCC_ST	<8,15,16,18,86>
+3VALW		+3VALW	<6,9,11,12,15,18,19,40,41,50,58,60,63,65,66,67,72,83,84,91,92,93,95>

TABLE of POWER SWITCH (U7101)		
Vendor	LCFC P/N	Description
TI	SA00008C900	S IC TPS22976DPUR WSON 14P LOAD SWITCH
GMT	SA00008F400	S IC G2898KD1U TDFN 14P LOAD SWITCH

### +1.05VALW to +VCC\_IO\_AP & +VCC\_ST



+5VALW		+5VALW	<38,39,41,42,43,47,62,64,66,67,71,84,85,86,87,88,89,91,93,94>
+5VS		+5VS	<41,47,50,51,60,61,65,66>
+3VALW		+3VALW	<6,9,11,12,15,18,19,40,41,50,58,60,63,65,66,67,71,83,84,91,92,93,95>
+3VS		+3VS	<5,9,10,11,12,14,15,23,25,30,32,37,39,40,47,50,57,58,59,60,63,65,66,67,69,82,85,86>
+3VL		+3VL	<19,40,42,67,80,82,83,84>
B+		B+	<47,60,80,83,84,85,86,87,88,89,91,92,95>



1. MIRROR code, is correct????
2. After reset EC, EC control "Low", not High or Disable.

# Smart Switch +5VALW To +5VS +3VALW To +3VS

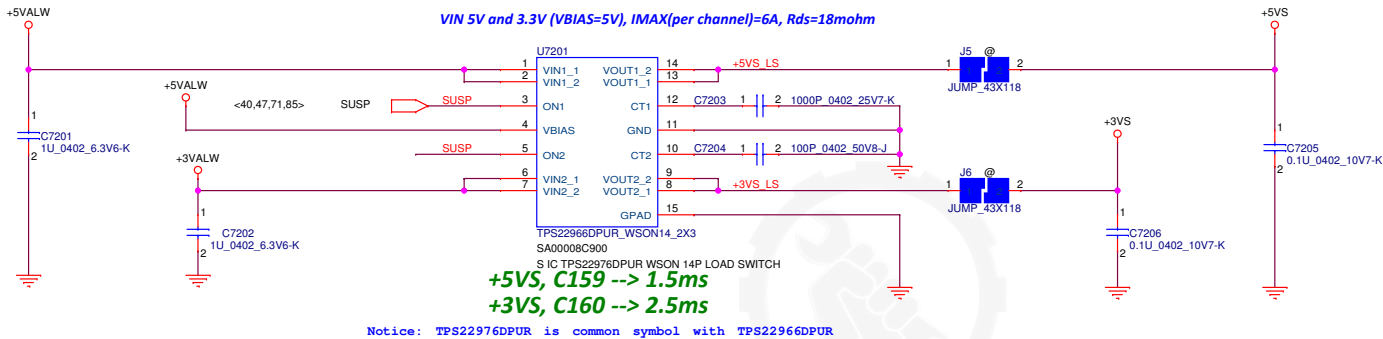
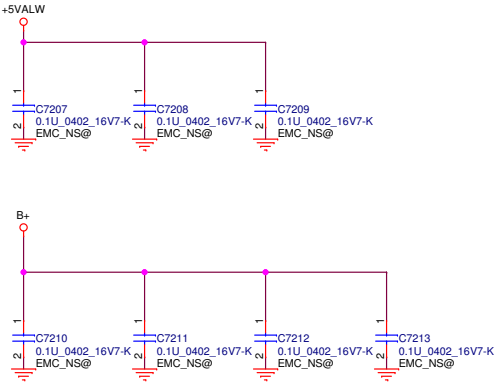



TABLE of POWER SWITCH (U7201)		
Vendor	LCFC P/N	Description
TI	SA00008C900	S IC TPS22976DPUR WSON 14P LOAD SWITCH
GMT	SA00008F400	S IC G2898KD1U TDFN 14P LOAD SWITCH



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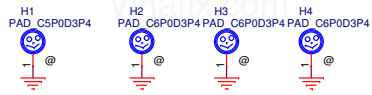


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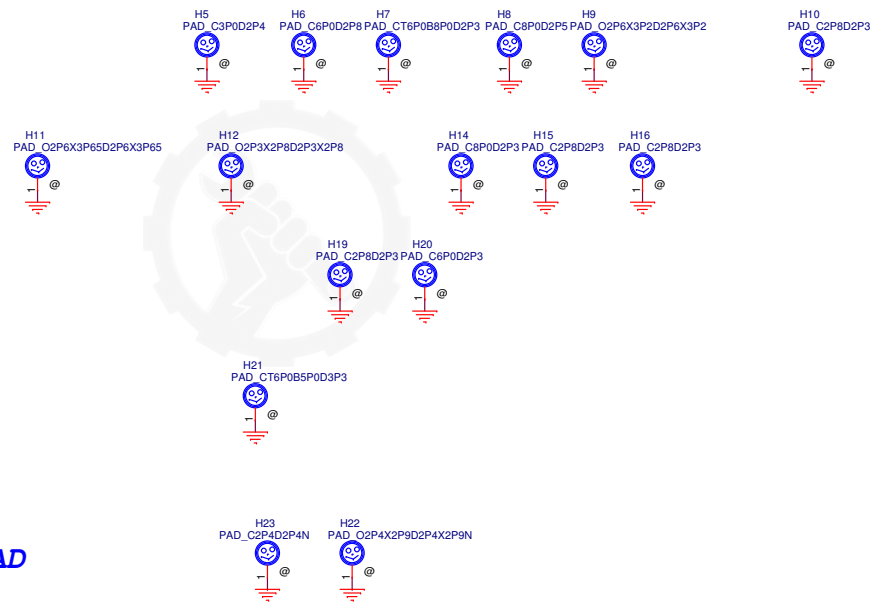


## Screw Hole

CPU




WLAN




## PCB Federal Mark PAD

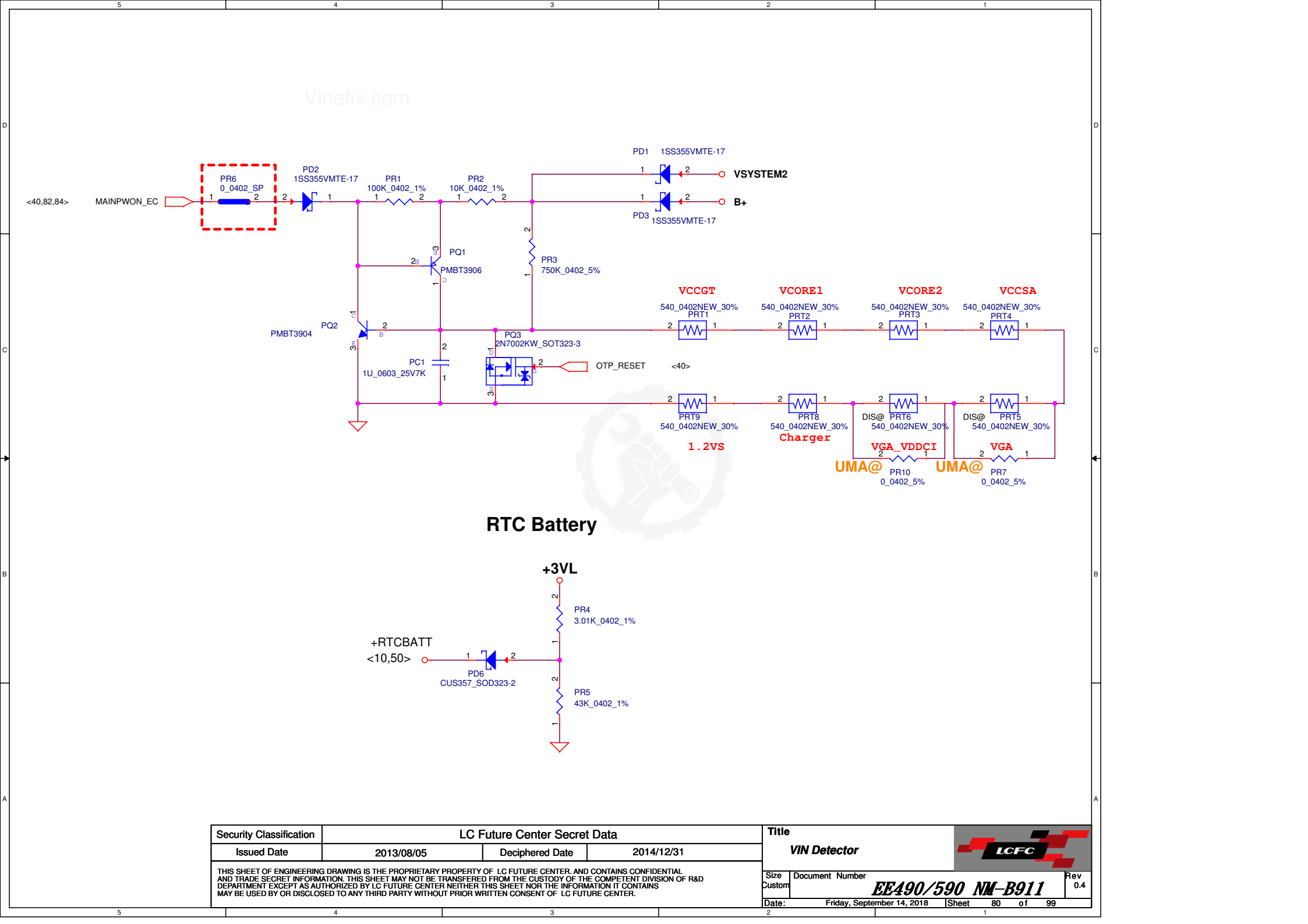


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<40,82,84>

MAINPWON\_EC

PR6  
0\_0402\_SP

PD2  
1SS355VMTE-17

PR1  
100K\_0402\_1%

PR2  
10K\_0402\_1%

PQ1  
PMBT3906

PQ2  
PMBT3904

PC1  
1U\_0603\_25V7K

PC2  
1U\_0603\_25V7K

PQ3  
2N7002KW\_SOT323-3

OTP\_RESET <40>

PR3  
750K\_0402\_5%

VSYSYSTEM2

B+

PD3  
1SS355VMTE-17

VCCGT  
540\_0402NEW\_30%  
PRT1

VCORE1  
540\_0402NEW\_30%  
PRT2

VCORE2  
540\_0402NEW\_30%  
PRT3

VCCSA  
540\_0402NEW\_30%  
PRT4

1.2VS  
540\_0402NEW\_30%  
PRT9

Charger  
540\_0402NEW\_30%  
PRT8

VGA\_VDDCI  
DIS@ PRT6  
540\_0402NEW\_30%

VGA  
DIS@ PRT5  
540\_0402NEW\_30%

UMA@ PR10  
0\_0402\_5%

UMA@ PR7  
0\_0402\_5%

**RTC Battery**

+3VL

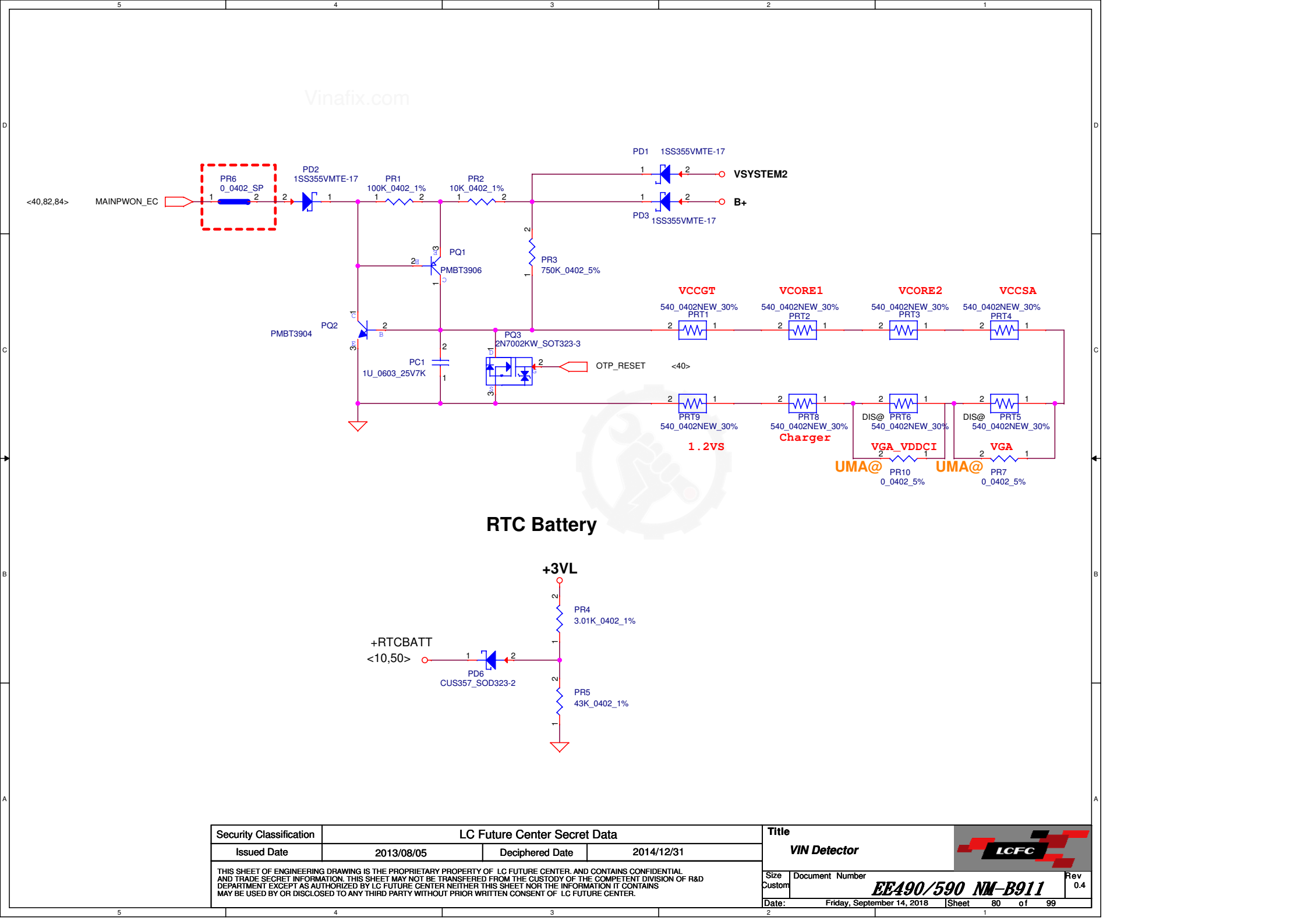
PR4  
3.01K\_0402\_1%

+RTCBATT <10,50>

PD6  
CUS357\_SOD323-2

PR5  
43K\_0402\_1%

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MAINPWON\_EC

PR6 0\_0402\_SP

PD2 1SS355VMTE-17

PR1 100K\_0402\_1%

PR2 10K\_0402\_1%

PQ1 PMBT3906

PQ2 PMBT3904

PC1 1U\_0603\_25V7K

PQ3 2N7002KW\_SOT323-3

PR3 750K\_0402\_5%

PD1 1SS355VMTE-17

PD3 1SS355VMTE-17

VSYSTEM2

B+

OTP\_RESET

1.2VS

VCCGT

VCORE1

VCORE2

VCCSA

UMA@

VGA\_VDDCI

VGA

UMA@

RTC Battery

+3VL

+RTCBATT

PR4 3.01K\_0402\_1%

PR5 43K\_0402\_1%


PD6 CUS357\_SOD323-2

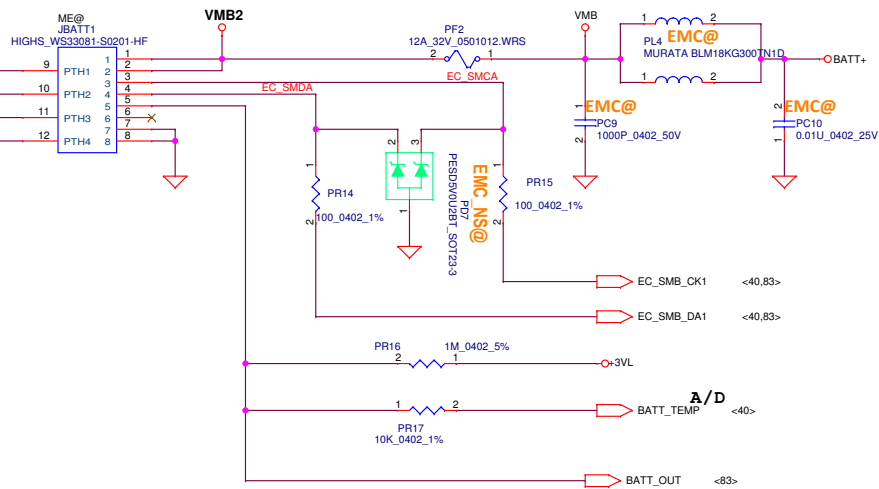
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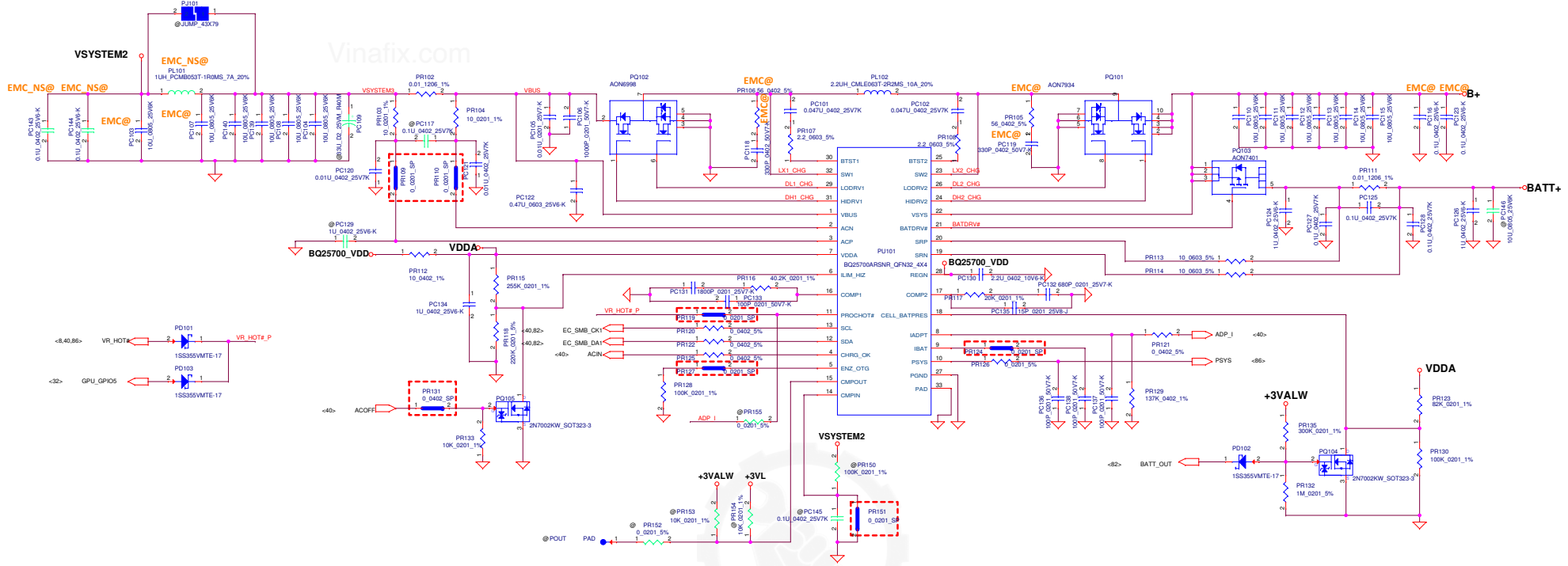
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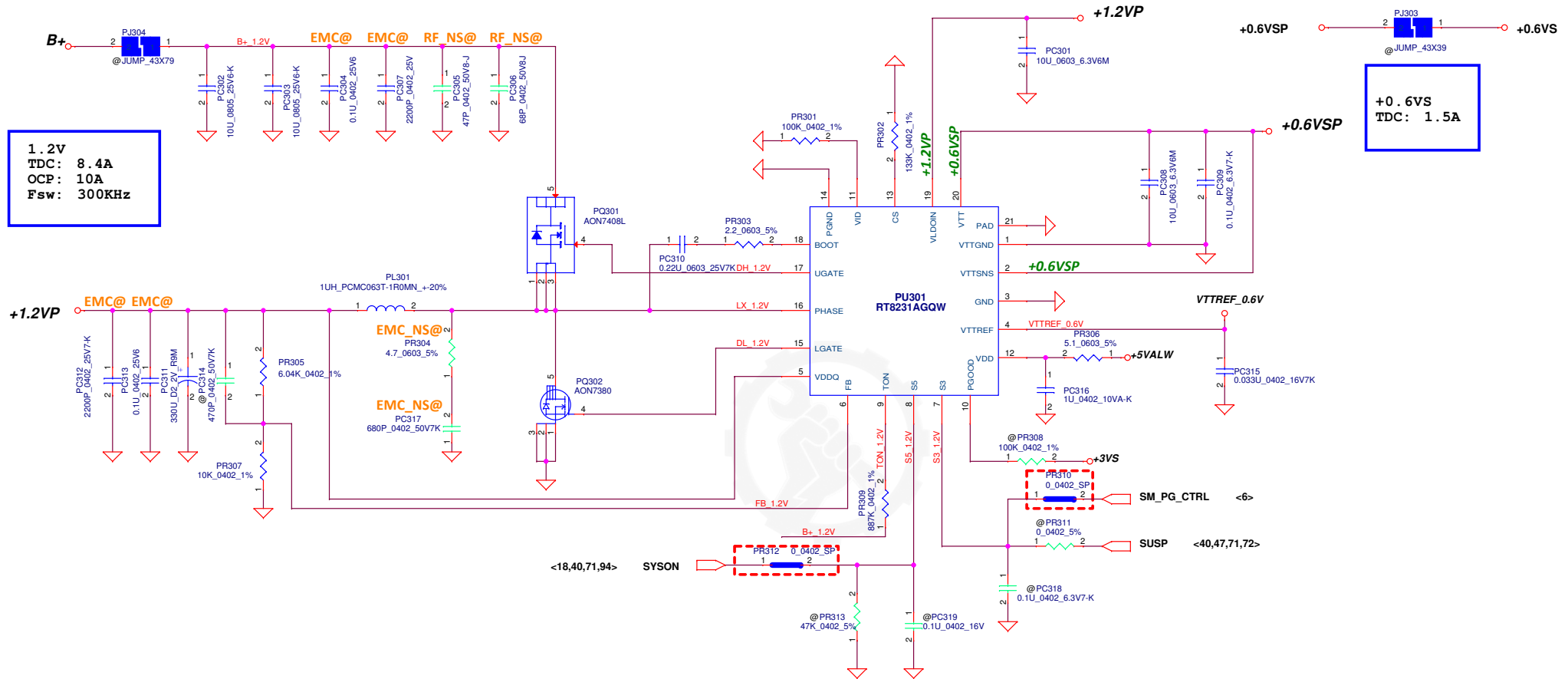
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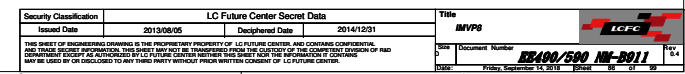


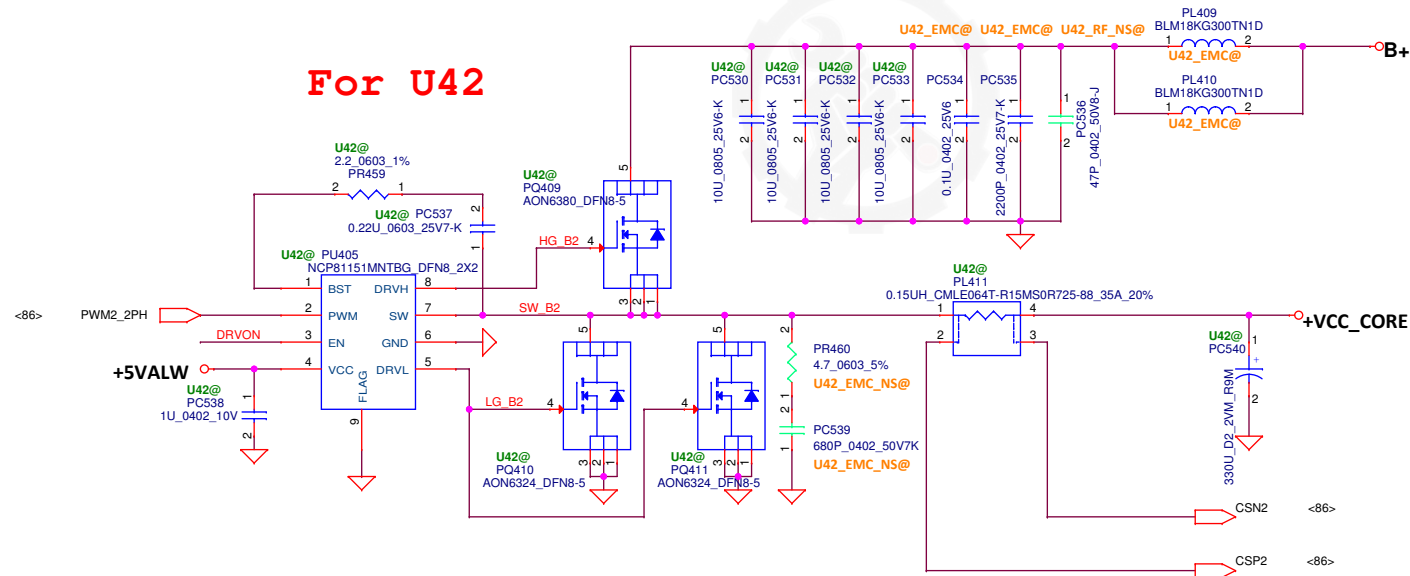
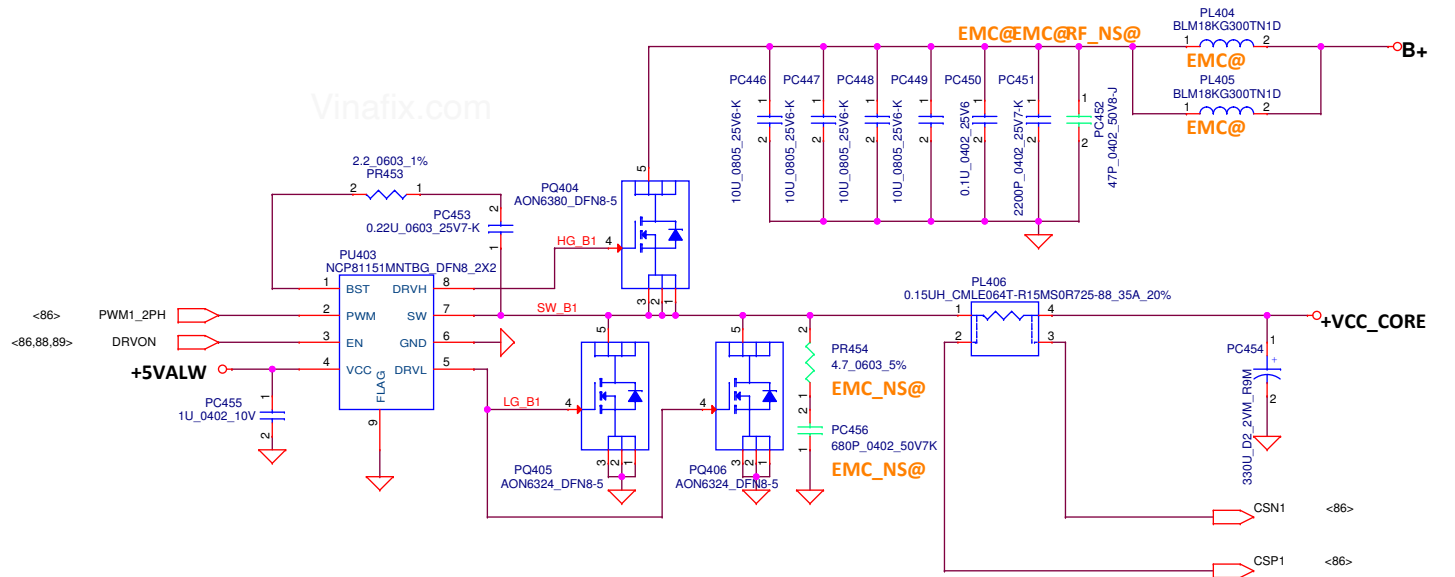




1.2V  
TDC: 8.4A  
OCP: 10A  
Fsw: 300KHz

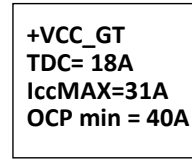
+0.6VS  
TDC: 1.5A





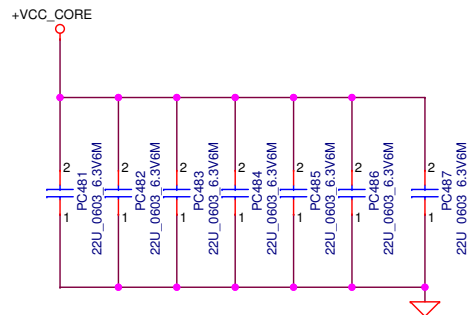
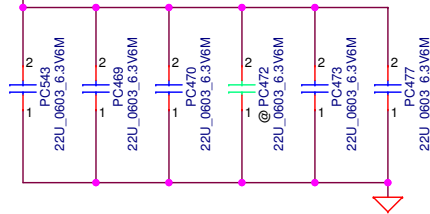
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Title			
+VCC_CORE			
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Custom			
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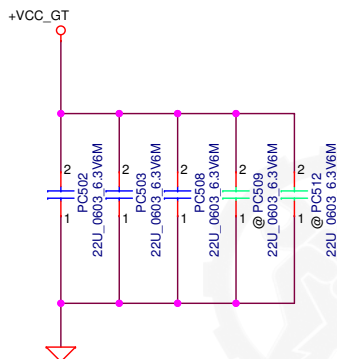
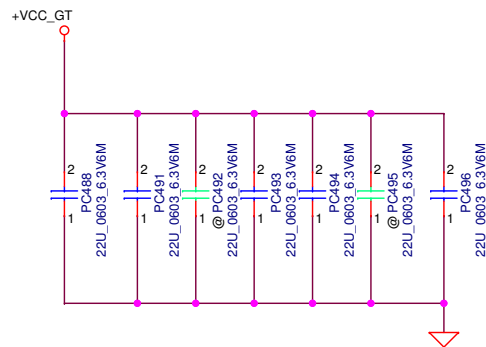




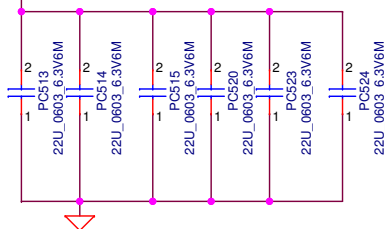
+VCC\_CORE  
12pcs 22uF for +VCC\_CORE



8pcs 22uF for +VCC\_GT



+VCC\_SA  
6pcs 22uF for +VCCSA

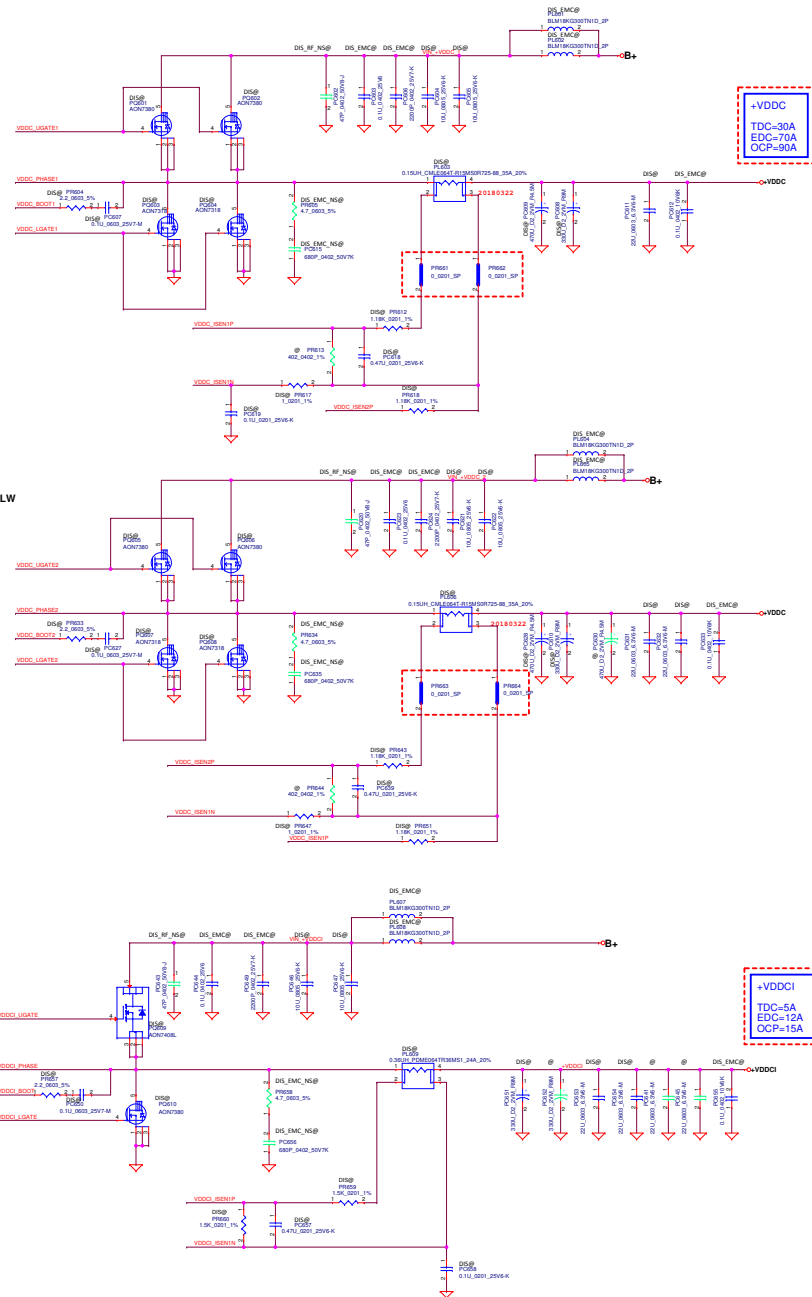
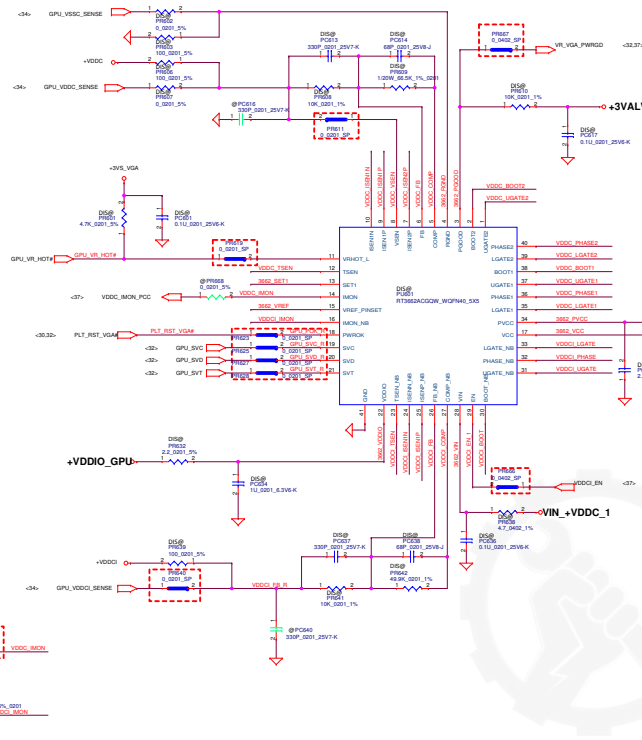



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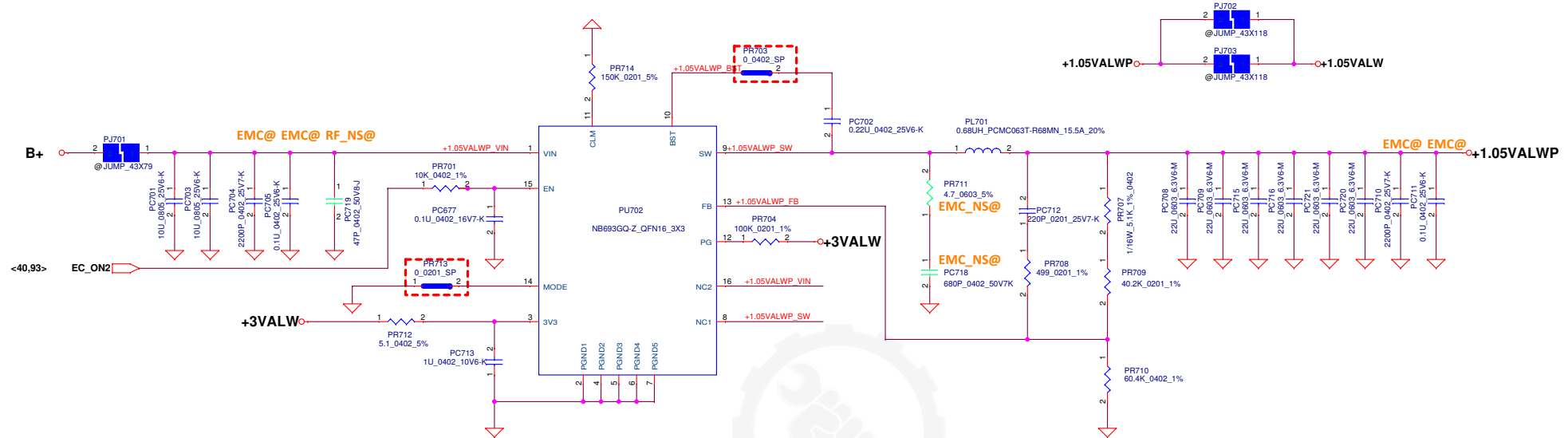
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PROCESSOR DECOUPLING			
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SVC	SVD	Boot Voltage
0	0	1.1V
0	1	1.0V
1	0	0.9V(Default)
1	1	0.8V

Timing diagram for GPU\_VSSC\_SENSE and VRL\_VGA\_PWNGO. The diagram shows a delay of 0.00015s between the two signals. A dashed red box highlights the VRL\_VGA\_PWNGO signal.

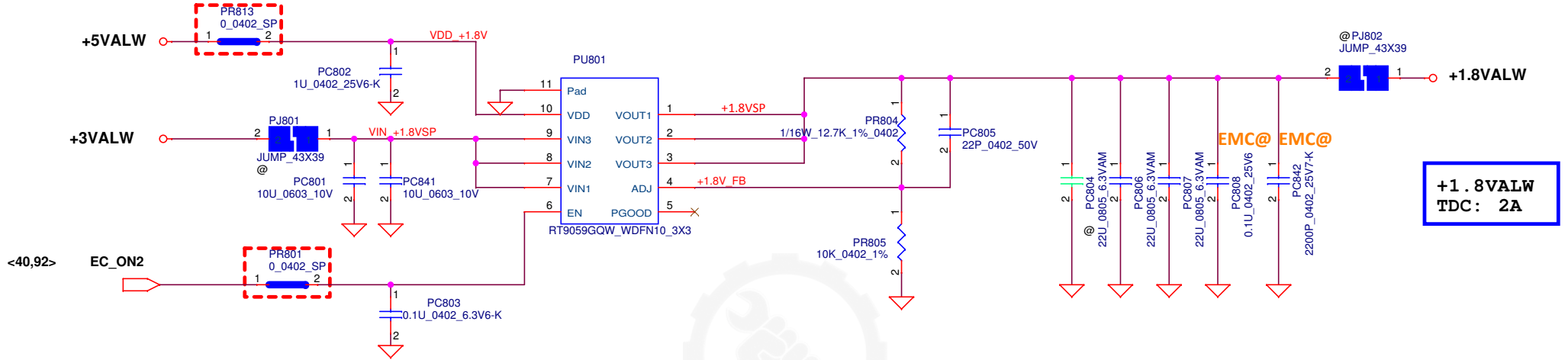


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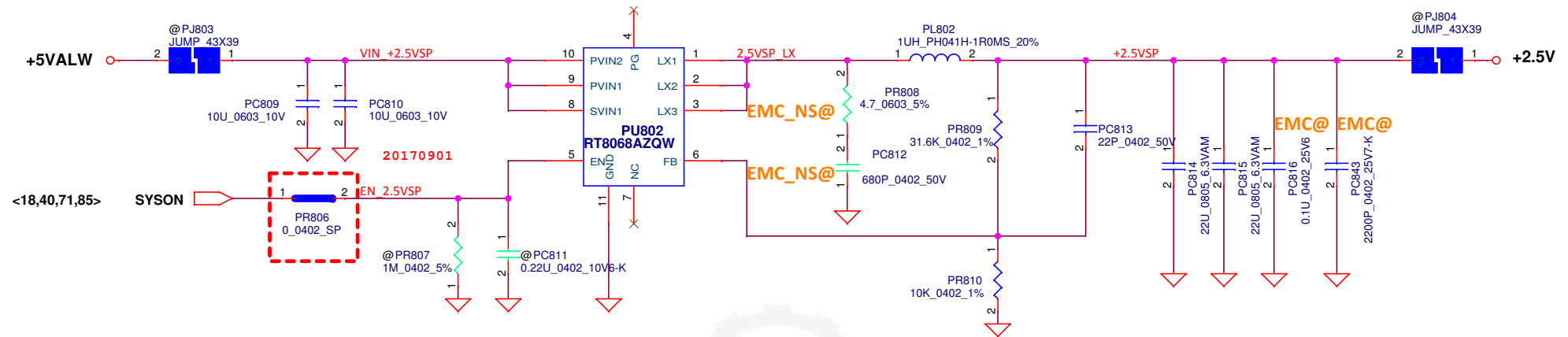



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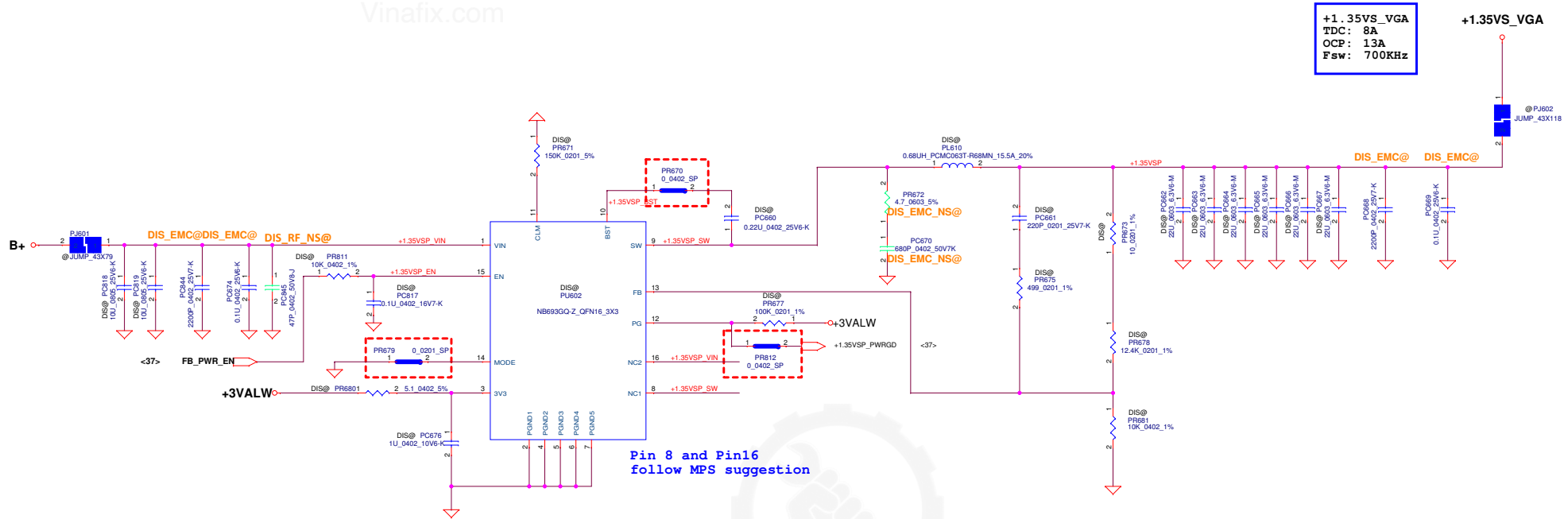




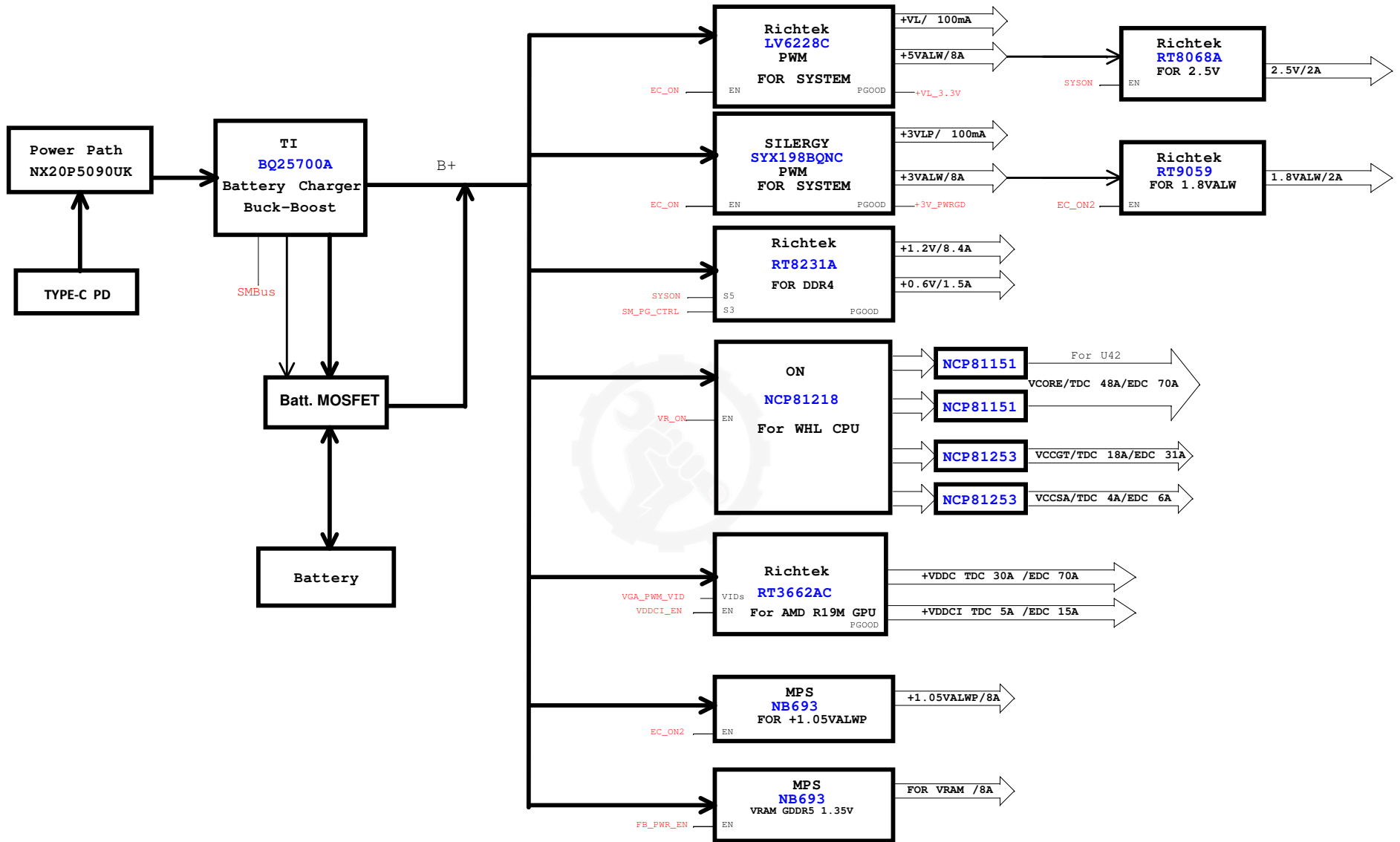
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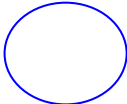
3

2

1

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PRTC2




BATT CR2032 3V 210MAH

RTC@

EE480



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# Power tree diagram



RTS5455 +LDO\_3V3, <40,42,43> TYPE-C

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